Applied Electronics

Instructor:

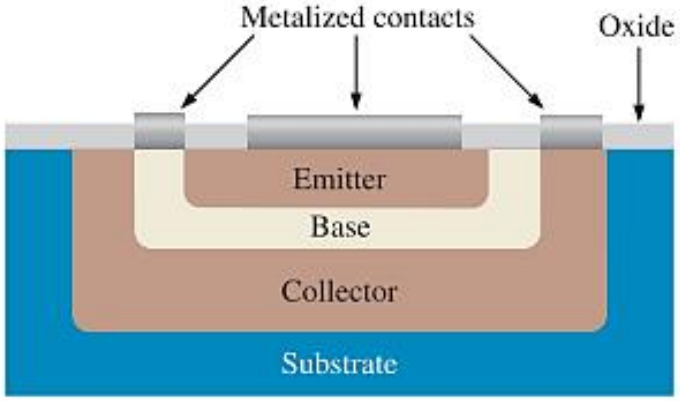
Dr. Ahmad El-Banna

DAY#2
SUMMER 2016

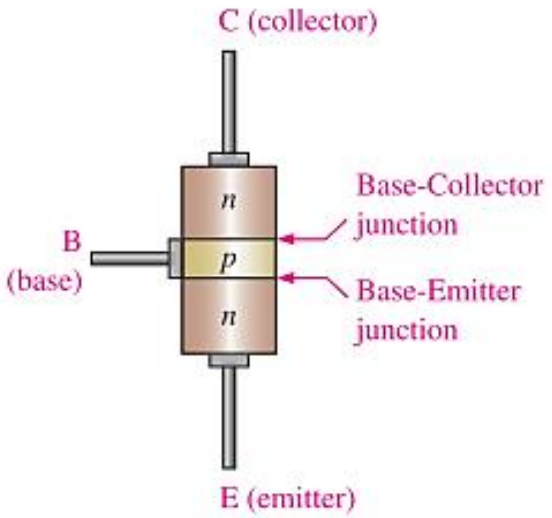
Agenda

- Transistors Structure
- Basic Operation
- Bias Circuits (DC Analysis)
- Models (AC Analysis)
- Troubleshooting
- Practical Applications

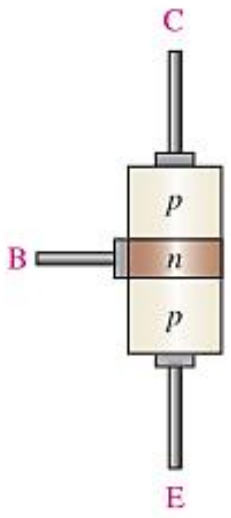
BIPOLAR JUNCTION TRANSISTOR (BJT) STRUCTURE



(a) Basic epitaxial planar structure

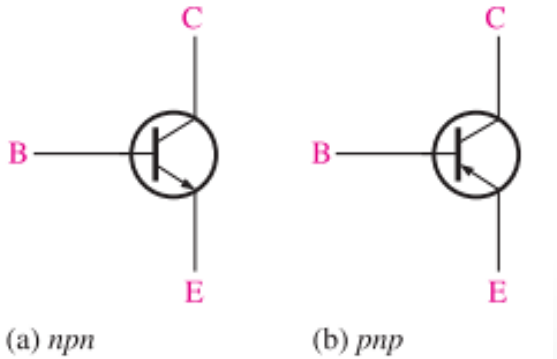


(b) *npn*



(c) *pnp*

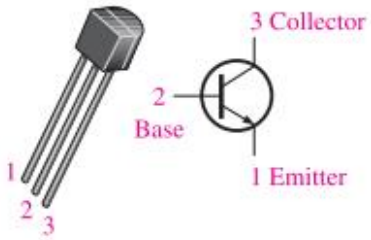
BJT symbol



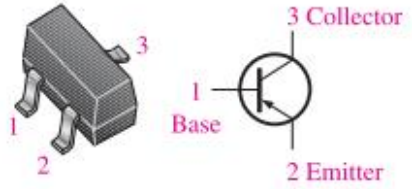
(a) *npn* (b) *pnp*

Transistor Packages

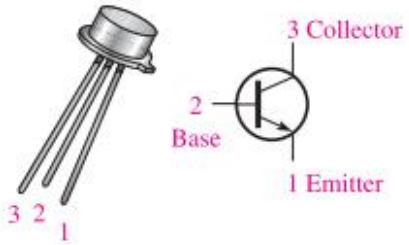
General Purpose



(a) TO-92

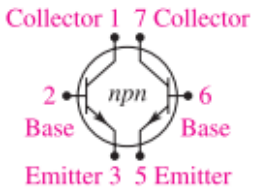


(b) SOT-23

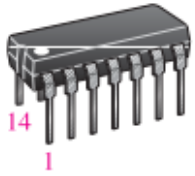


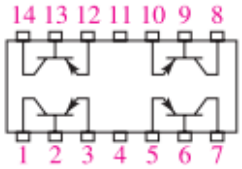
(c) TO-18. Emitter is closest to tab.

Multiple Transistor Package

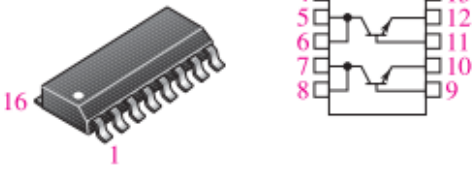


(a) Dual metal can. Emitters are closest to tab.



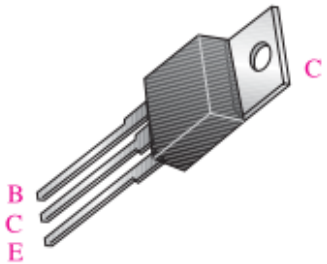


(b) Quad dual in-line (DIP) and quad flat-pack. Dot indicates pin 1.

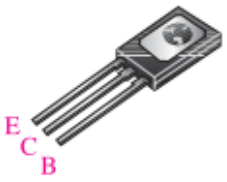


(c) Quad small outline (SO) package for surface-mount technology

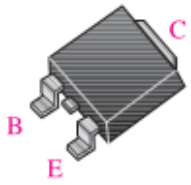
Power Transistors



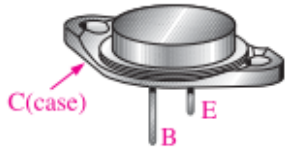
(a) TO-220



(b) TO-225



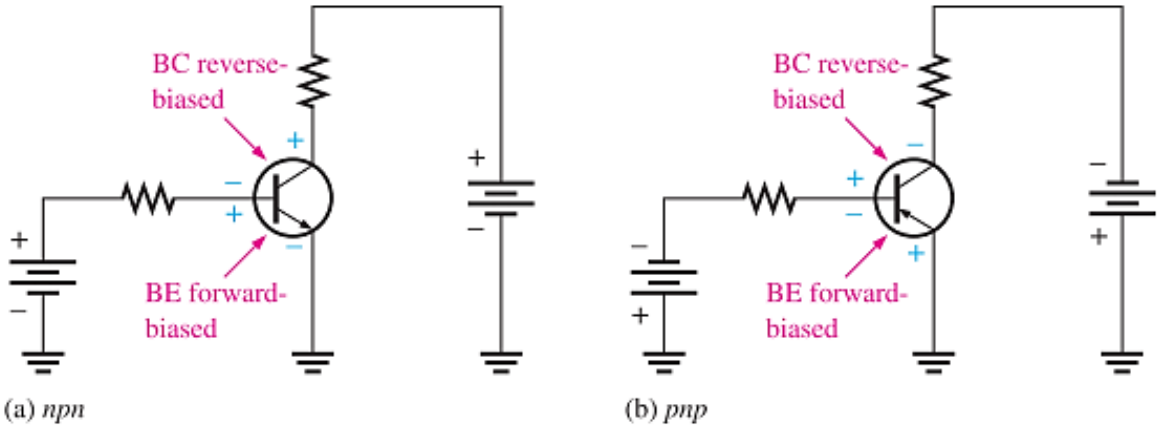
(c) D-Pack



(d) TO-3

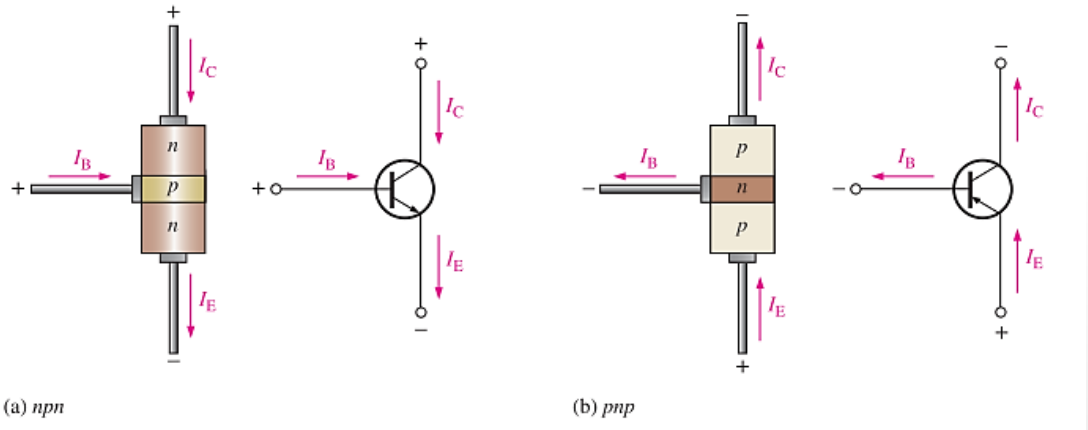
Basic Operation

- **Biasing & Operation**



- **Transistor Currents**

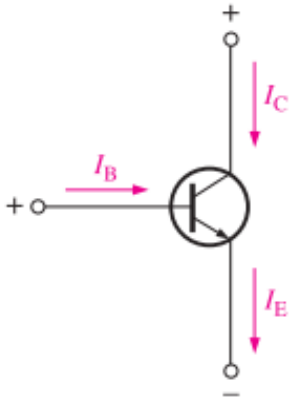
$$I_E = I_C + I_B$$



BJT Configurations

Configuration	Input	Output
Common Emitter	Base	Collector
Common Base	Emitter	Collector
Common Collector	Base	Emitter

- Base terminal can't be output
- Collector terminal can't be input



BJT Parameters

$$\beta_{DC} = \frac{I_C}{I_B}$$

- The dc current gain of a transistor is the ratio of the dc collector current (I_C) to the dc base current (I_B) and is designated dc **beta** (β_{DC}).

$$h_{FE} = \beta_{DC}$$

- Typical values of β_{DC} range from less than 20 to 200 or higher.
- β_{DC} is usually designated as an equivalent hybrid (h) parameter, h_{FE}, on transistor datasheets.

$$\alpha_{DC} = \frac{I_C}{I_E}$$

- The ratio of the dc collector current (I_C) to the dc emitter current (I_E) is the dc alpha (α_{DC}).

Transistor DC Model

I_B: dc base current

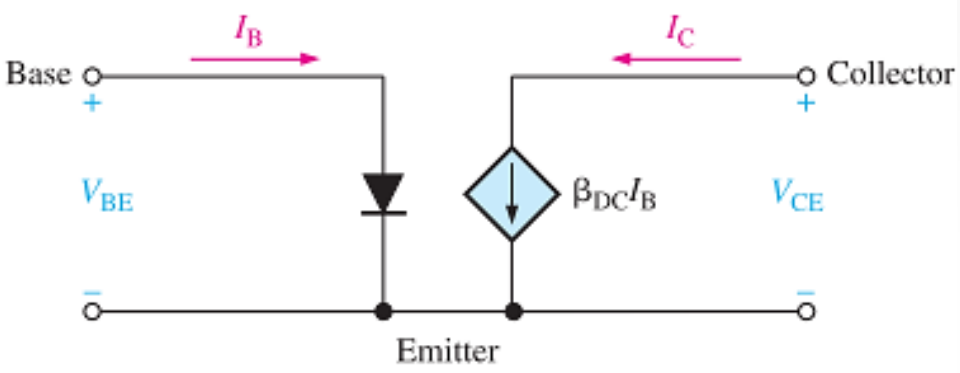
I_E: dc emitter current

I_C: dc collector current

V_{BE}: dc voltage at base with respect to emitter

V_{CB}: dc voltage at collector with respect to base

V_{CE}: dc voltage at collector with respect to emitter



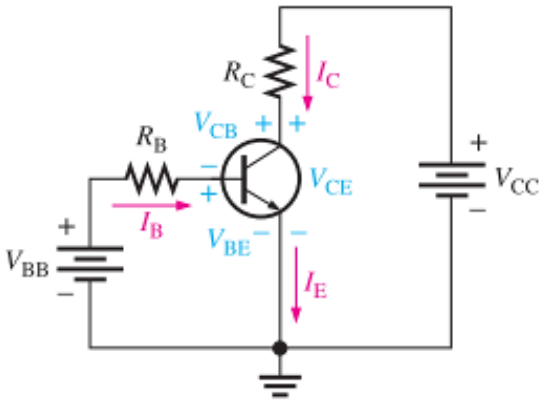
$$V_{BE} \cong 0.7\,\text{V}$$

$$V_{R_B} = V_{BB} - V_{BE}$$

$$V_{R_B} = I_B R_B$$

$$I_B R_B = V_{BB} - V_{BE}$$

$$I_B = \frac{V_{BB} - V_{BE}}{R_B}$$



$$V_{CE} = V_{CC} - V_{R_C}$$

$$V_{R_C} = I_C R_C$$

$$I_c = \beta I_B$$

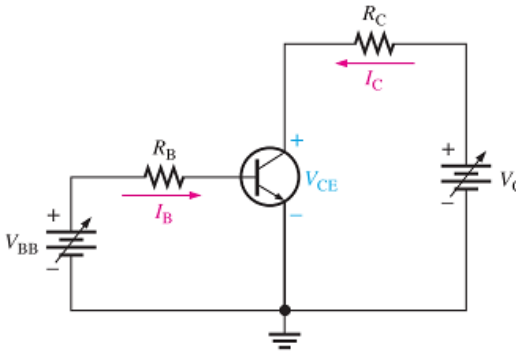
$$V_{CE} = V_{CC} - I_C R_C$$

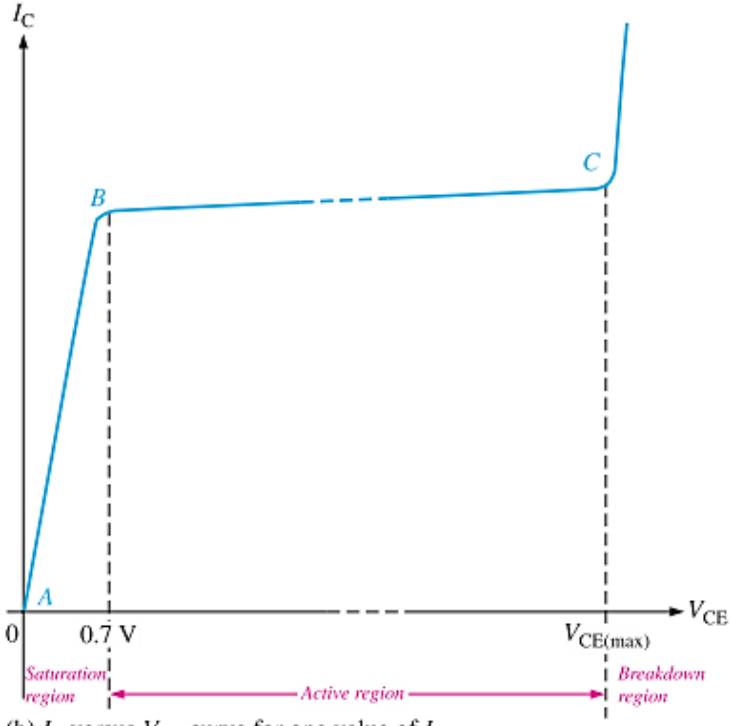
$$V_{CB} = V_{CE} - V_{BE}$$

Collector characteristic curves

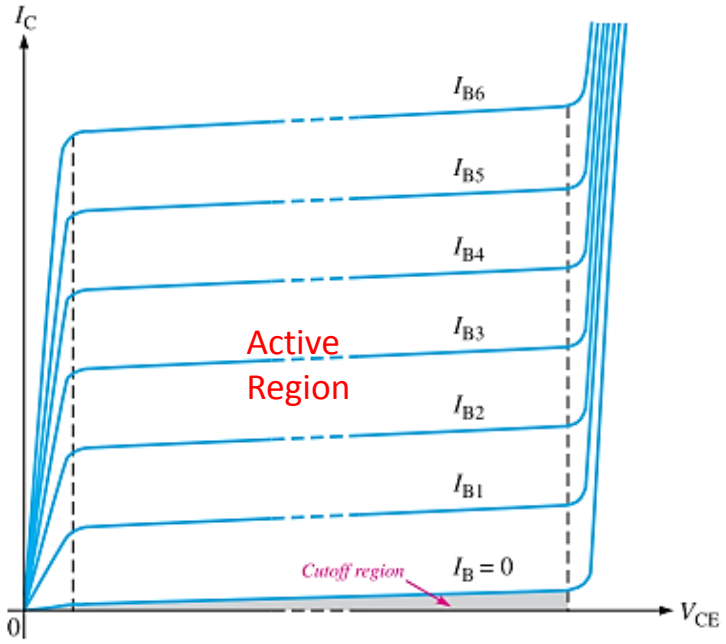
Operation Regions

- Active
- Cut-off
- Saturation



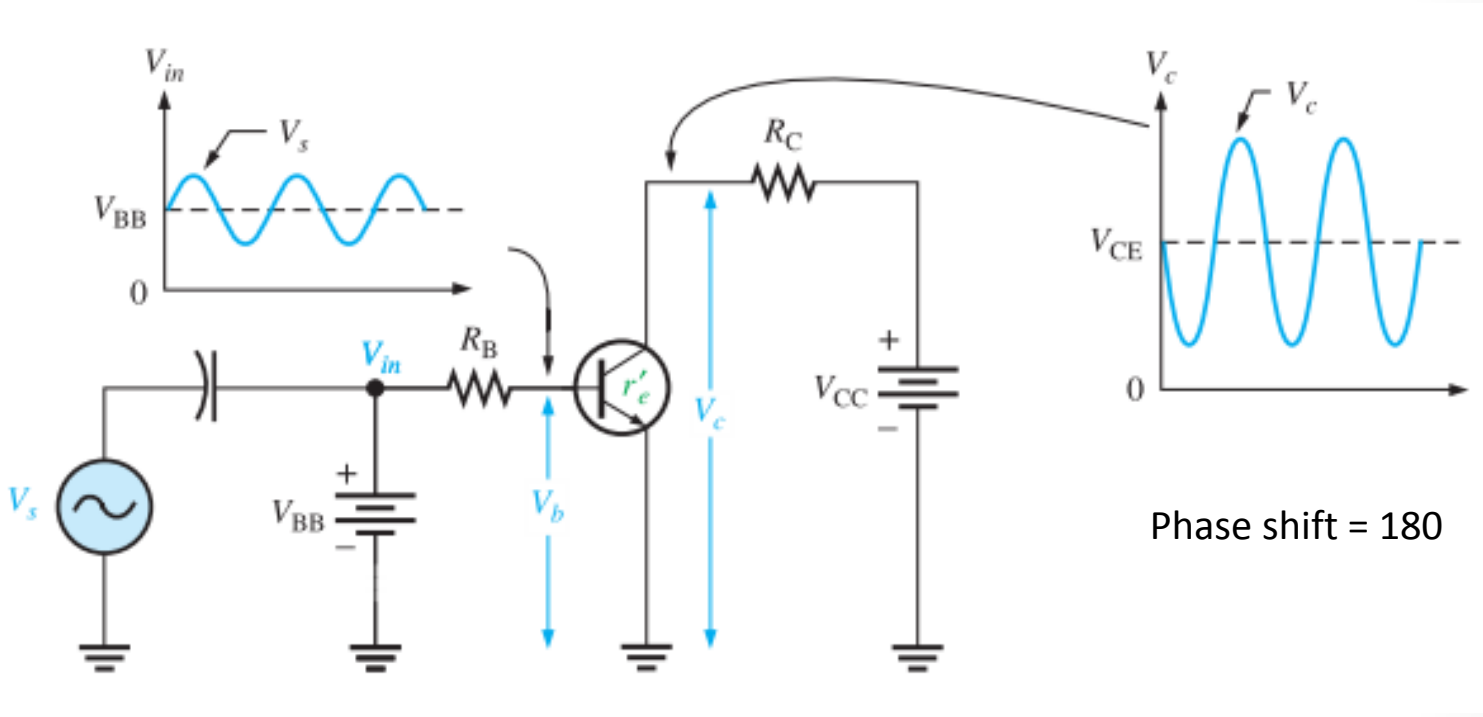


(b) I_C versus V_{CE} curve for one value of I_B



(c) Family of I_C versus V_{CE} curves for several values of I_B ($I_{B1} < I_{B2} < I_{B3}$, etc.)

BJT as an Amplifier



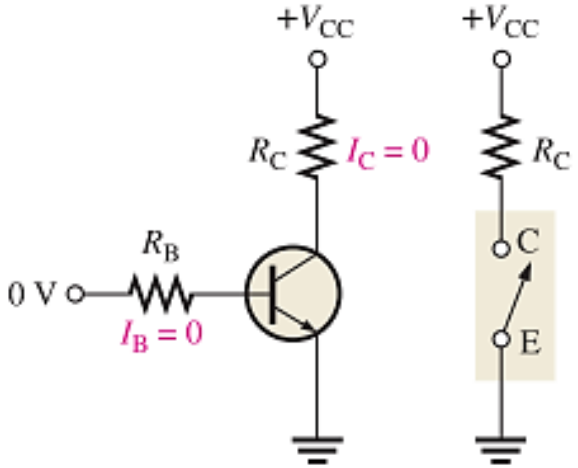
Phase shift = 180

Voltage gain magnitude: $A_v \cong \frac{R_C}{r'_e}$

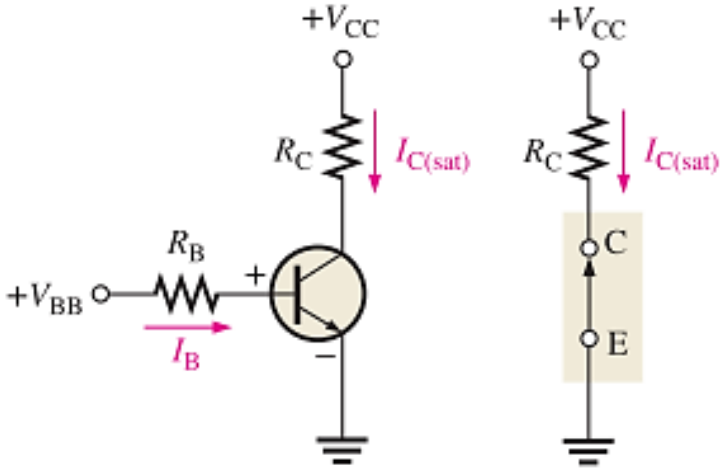
$r_e = 26\ mv / I_E$

$I_E = I_C + I_B$

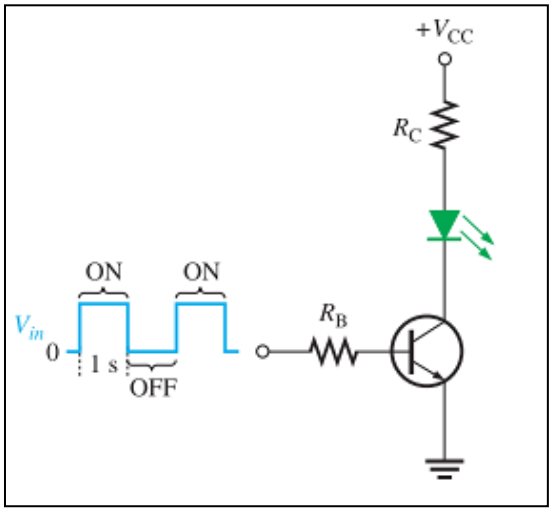
BJT as a Switch



(a) Cutoff — open switch

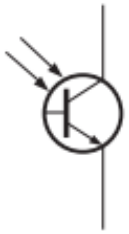


(b) Saturation — closed switch

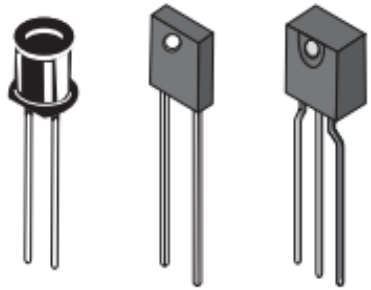


The Phototransistor

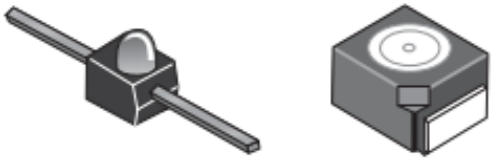
$$I_C = \beta_{DC} I_\lambda$$

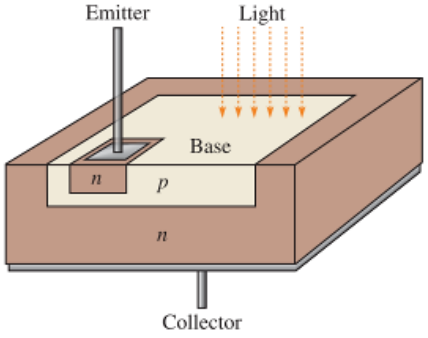


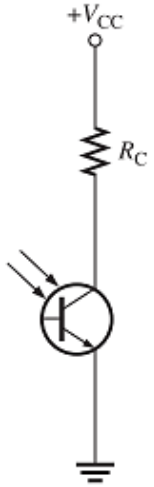
(a) Schematic symbol

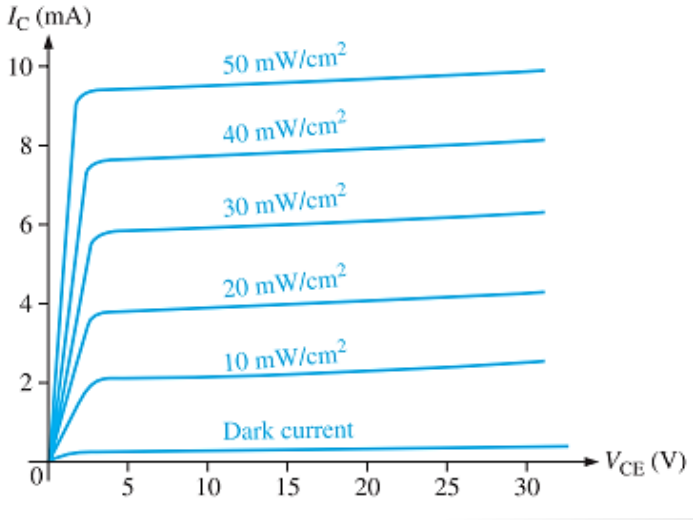


(b) Typical packages



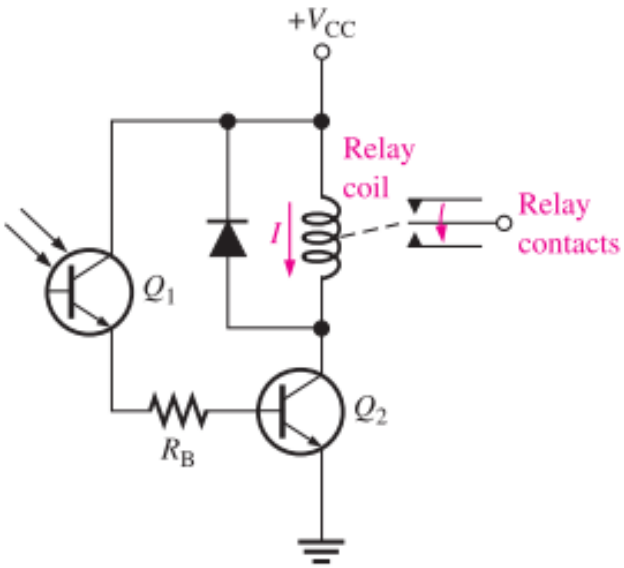




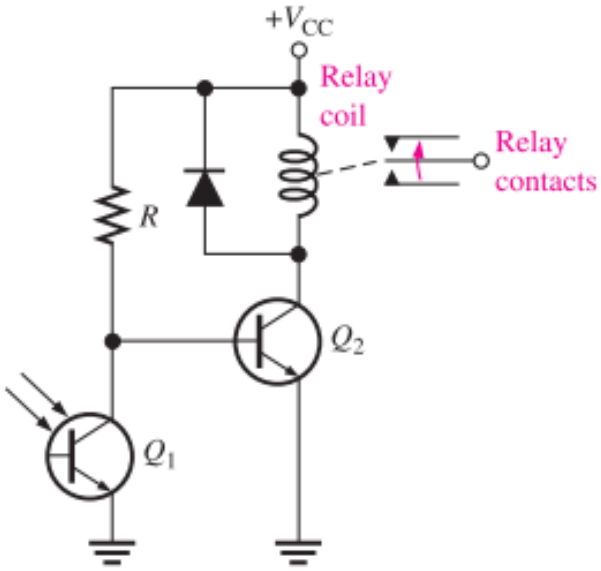


Phototransistor Application

Relay circuits driven by a phototransistor



(a) Light activated

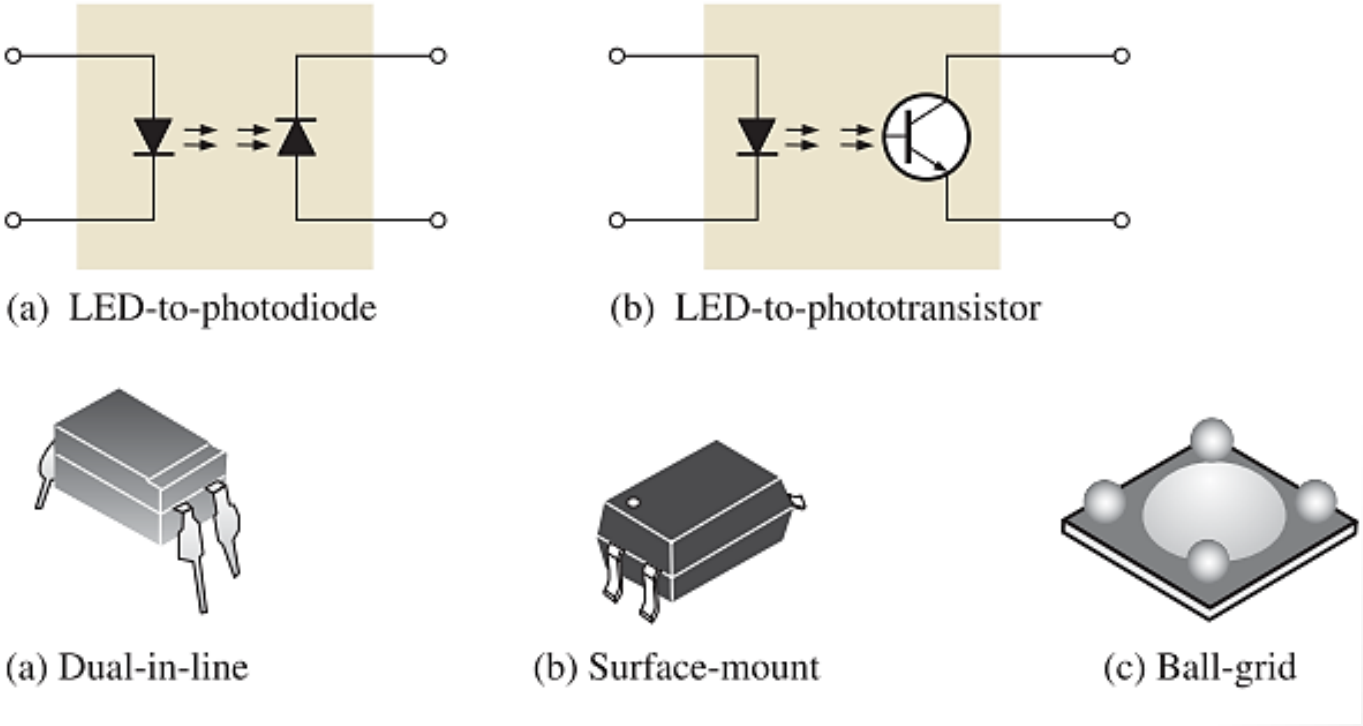


(b) Light deactivated

- A **relay** is an electrically operated switch.
- **relays** use an electromagnet to mechanically operate a switch

Optocouplers

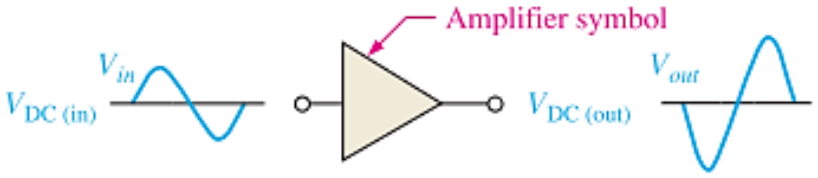
- **Basic optocouplers**



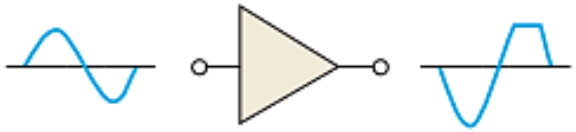
Examples of optocoupler packages

Transistor Bias Circuit

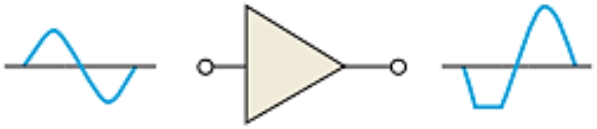
- What's Biasing?
  - Bias establishes the dc operating point (Q-point) for proper linear operation of an amplifier.
- Why?
  - If an amplifier is not biased with correct dc voltages on the input and output, it can go into saturation or cutoff when an input signal is applied.



(a) Linear operation: larger output has same shape as input except that it is inverted

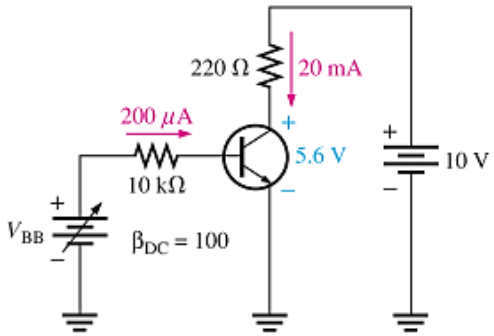


(b) Nonlinear operation: output voltage limited (clipped) by cutoff

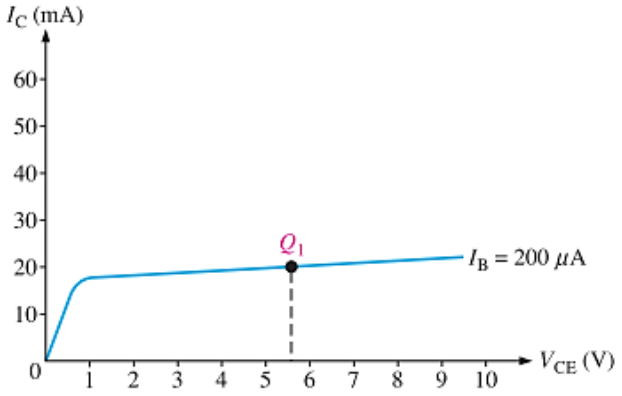


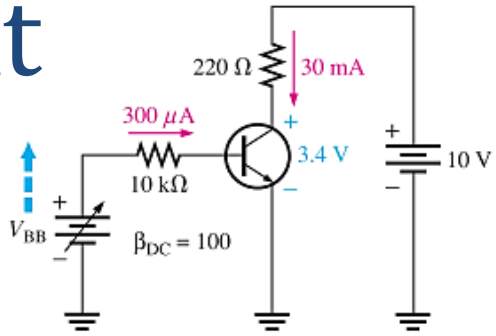
(c) Nonlinear operation: output voltage limited (clipped) by saturation

Q-point Adjustment

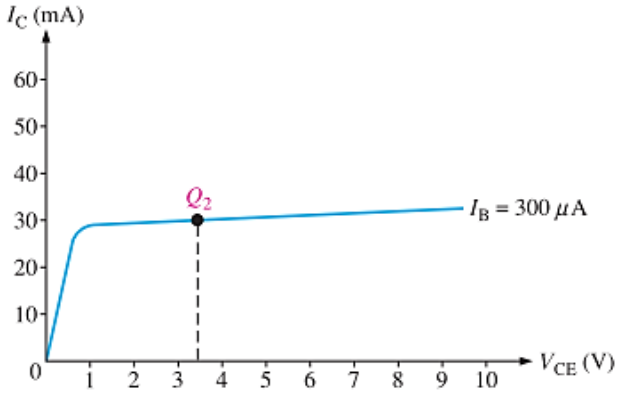


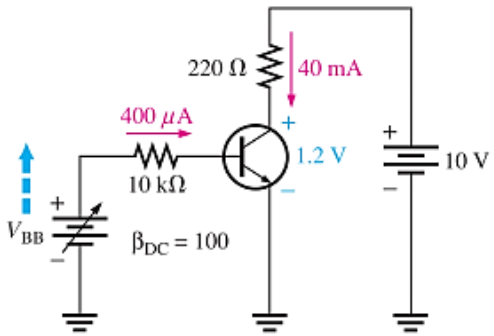
(a) $I_B = 200\ \mu A$



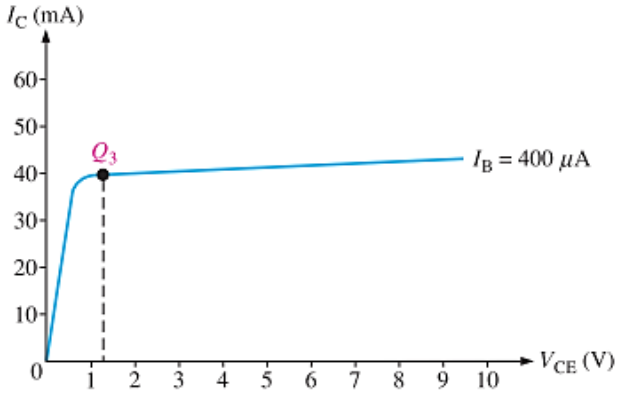


(b) Increase I_B to 300 μA by increasing V_{BB}

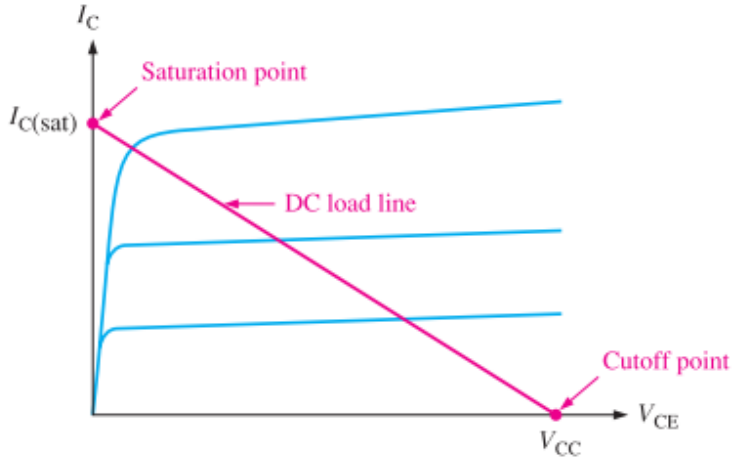


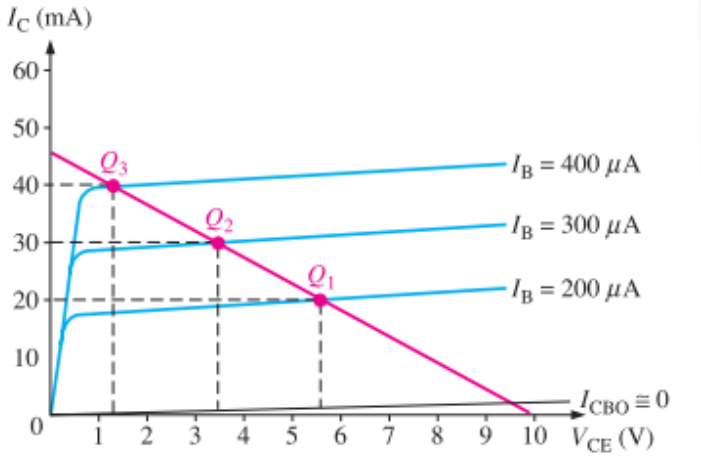


(c) Increase I_B to 400 μA by increasing V_{BB}

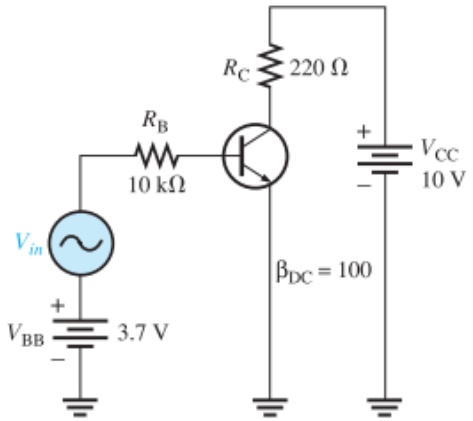


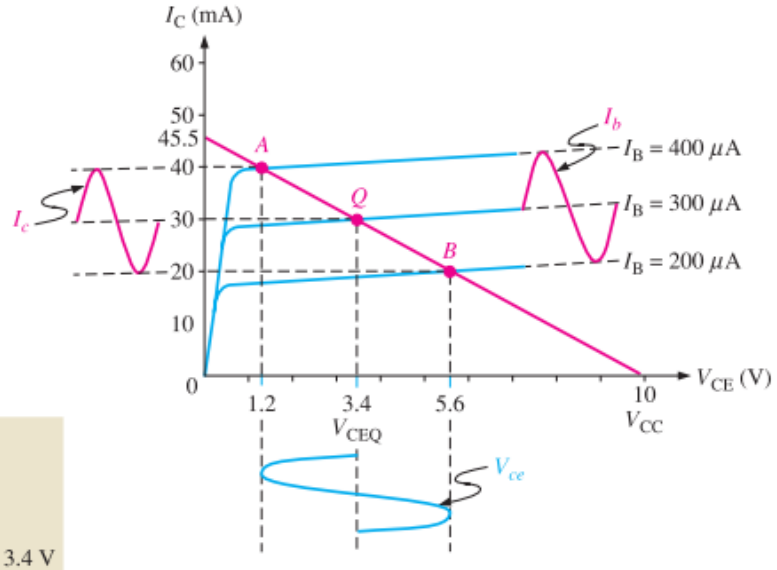
DC Load Line





- Variations in collector current and collector-to-emitter voltage as a result of a variation in base current.



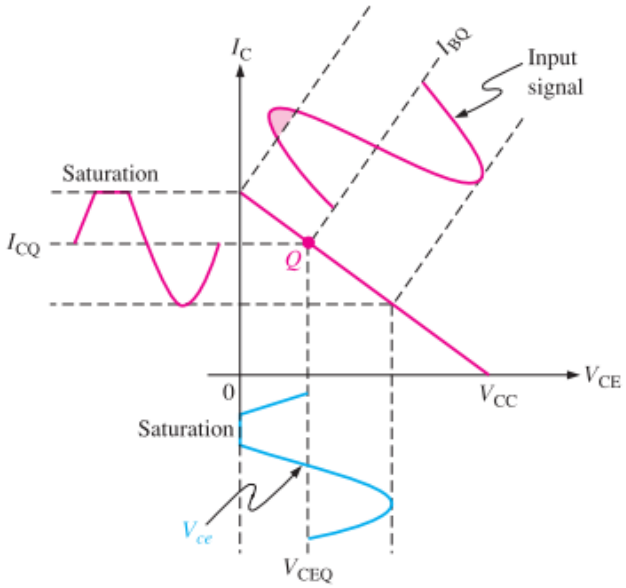


$$I_{BQ} = \frac{V_{BB} - 0.7\ V}{R_B} = \frac{3.7\ V - 0.7\ V}{10\ k\Omega} = 300\ \mu A$$

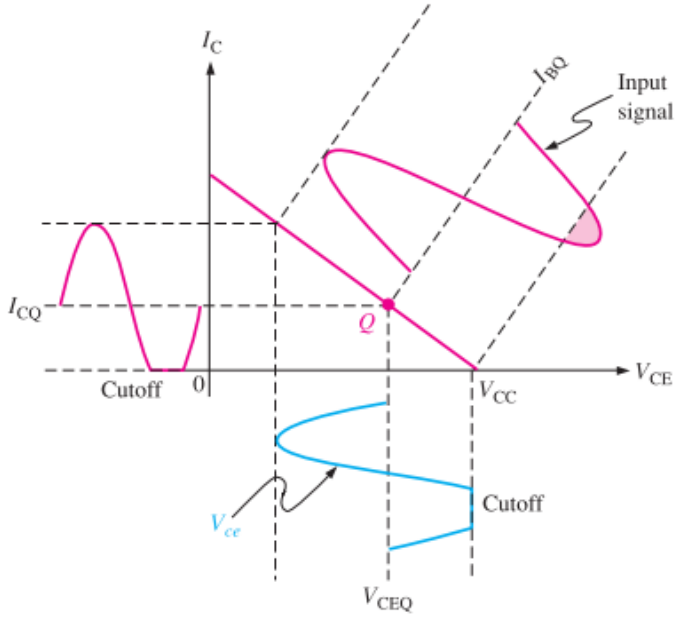
$$I_{CQ} = \beta_{DC} I_{BQ} = (100)(300\ \mu A) = 30\ mA$$

$$V_{CEQ} = V_{CC} - I_{CQ} R_C = 10\ V - (30\ mA)(220\ \Omega) = 3.4\ V$$

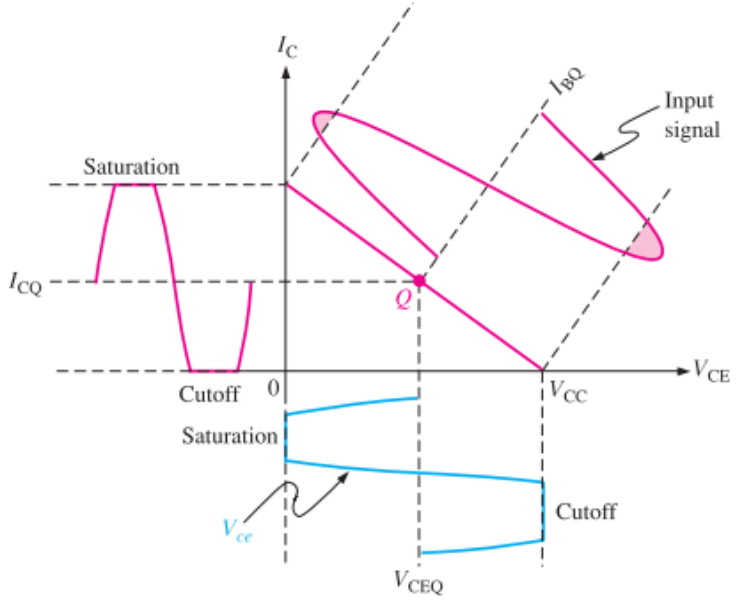
Waveform Distortion



(a) Transistor is driven into saturation because the Q-point is too close to saturation for the given input signal.

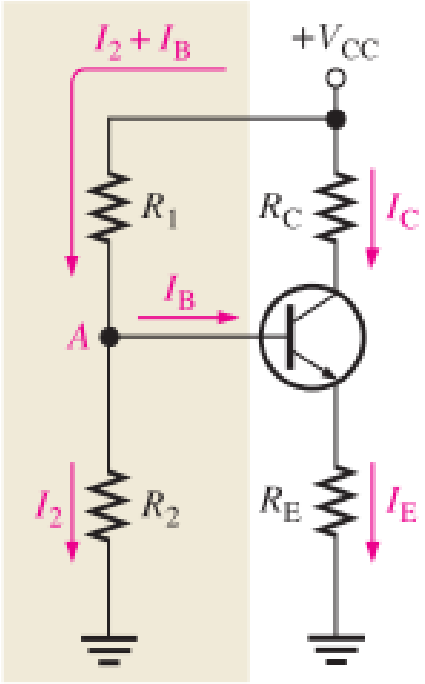


(b) Transistor is driven into cutoff because the Q-point is too close to cutoff for the given input signal.



(c) Transistor is driven into both saturation and cutoff because the input signal is too large.

VOLTAGE-DIVIDER BIAS



$$V_B \cong \left(\frac{R_2}{R_1 + R_2}\right)V_{CC}$$

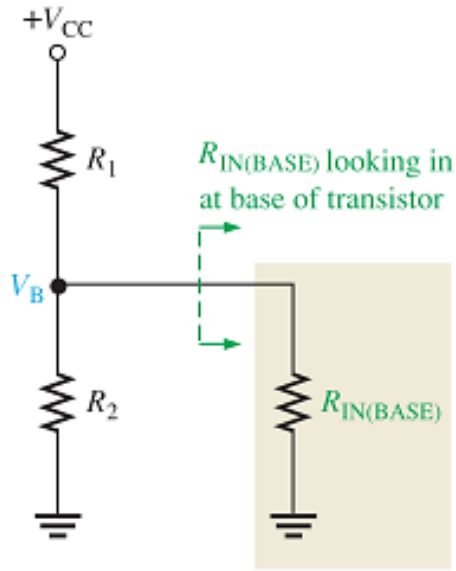
$$V_E = V_B - V_{BE}$$

$$I_C \cong I_E = \frac{V_E}{R_E}$$

$$V_C = V_{CC} - I_C R_C$$

$$V_{CE} = V_C - V_E$$

Loading Effects of Voltage-Divider Bias



Stiff:

$$R_{IN(BASE)} \cong 10R_2$$

$$V_B \cong \left(\frac{R_2}{R_1 + R_2}\right) V_{CC}$$

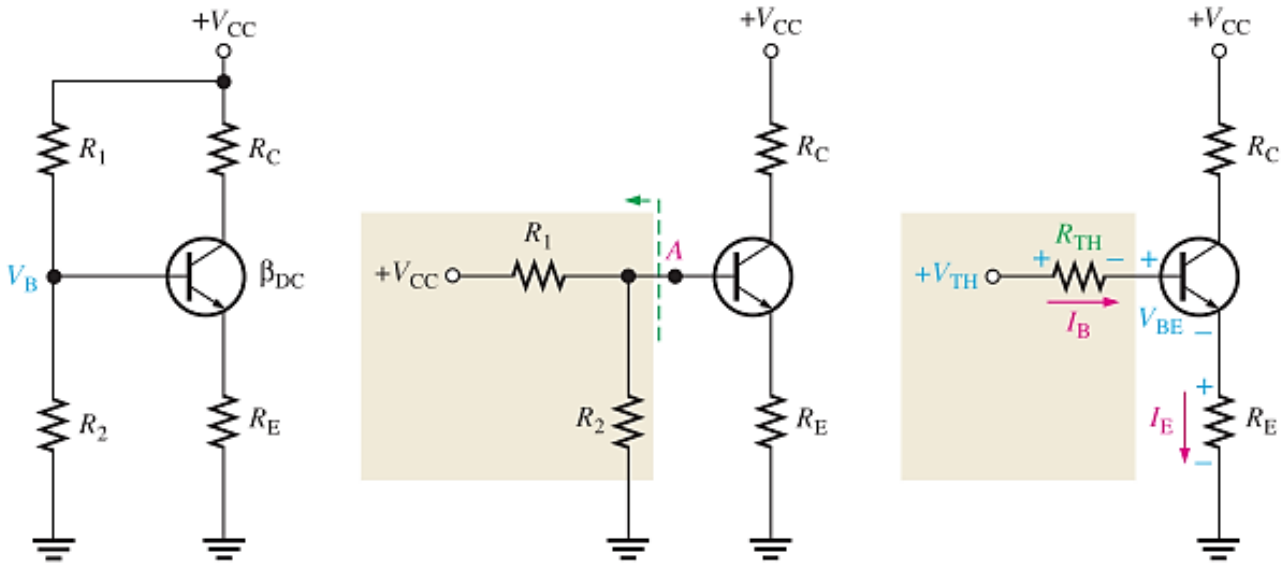
Not stiff:

$$R_{IN(BASE)} < 10R_2$$

$$V_B = \left(\frac{R_2 \parallel R_{IN(BASE)}}{R_1 + R_2 \parallel R_{IN(BASE)}}\right) V_{CC}$$

$$R_{IN(BASE)} = \frac{\beta_{DC} V_B}{I_E}$$

Thevenin's Theorem Applied to Voltage-Divider Bias



$$V_{TH} = \left(\frac{R_2}{R_1 + R_2}\right)V_{CC}$$

$$R_{TH} = \frac{R_1 R_2}{R_1 + R_2}$$

$$V_{TH} - V_{R_{TH}} - V_{BE} - V_{R_E} = 0$$

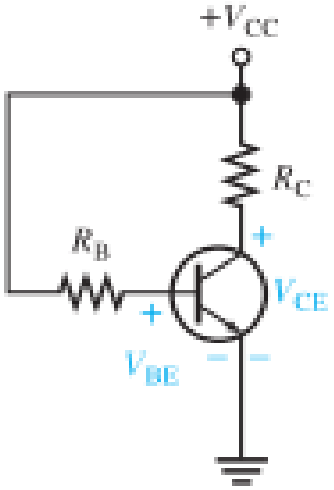
$$V_{TH} = I_B R_{TH} + V_{BE} + I_E R_E$$

$$V_{TH} = I_E(R_E + R_{TH}/\beta_{DC}) + V_{BE}$$

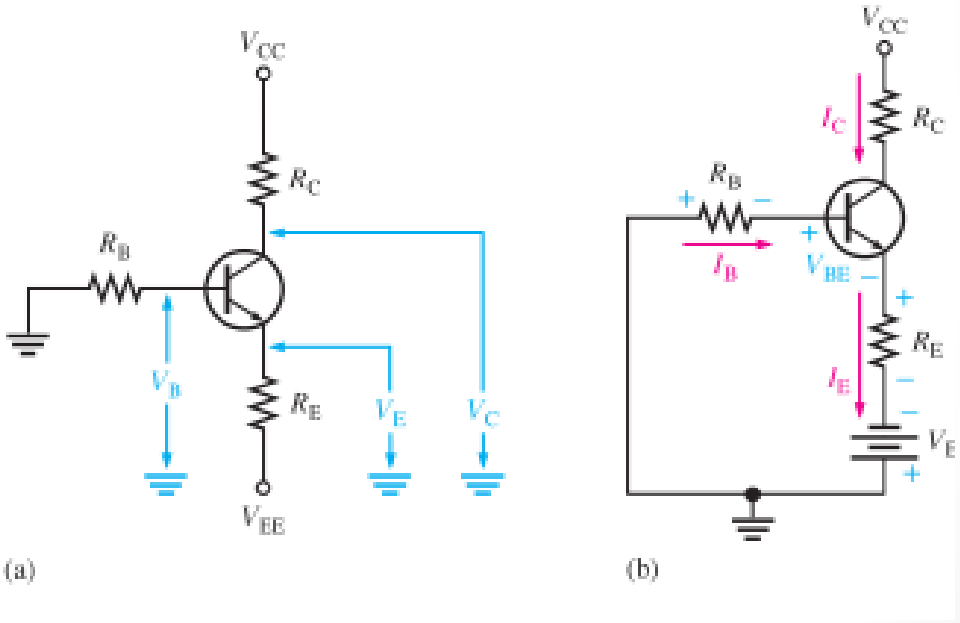
$$I_E = \frac{V_{TH} - V_{BE}}{R_E + R_{TH}/\beta_{DC}}$$

Other Bias Circuits

Base Bias

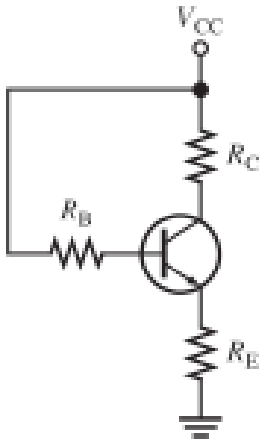


Emitter Bias

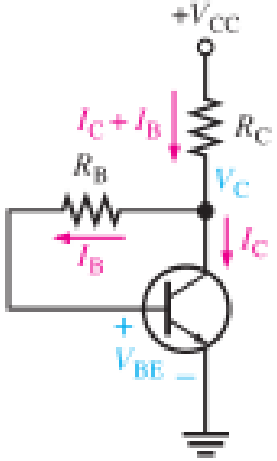


Other Bias Circuits..

Emitter Feedback Bias



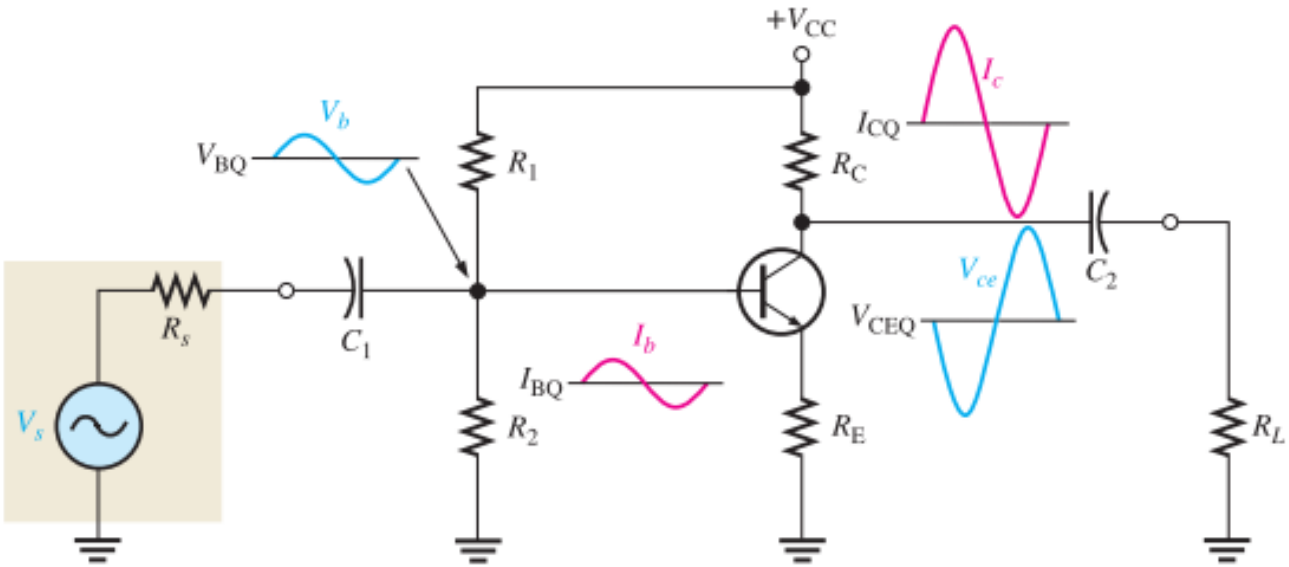
Collector Feedback Bias

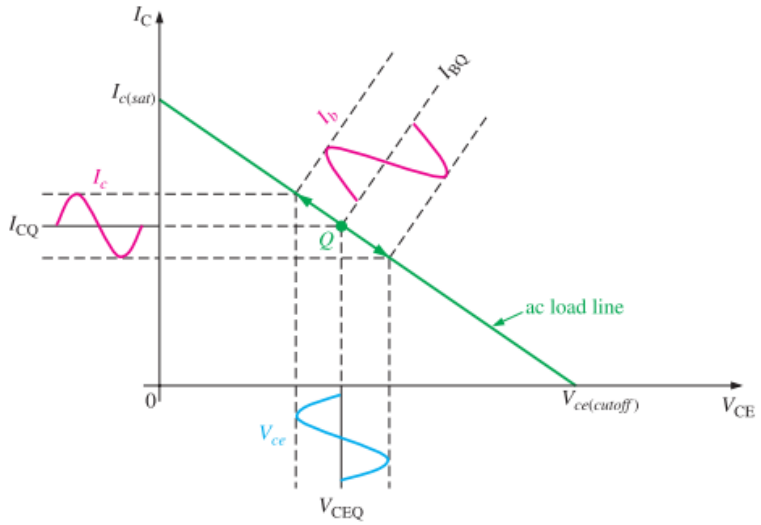


Note:

Different bias circuits has different stability levels against beta and/or temperature changes

Linear Amplifier





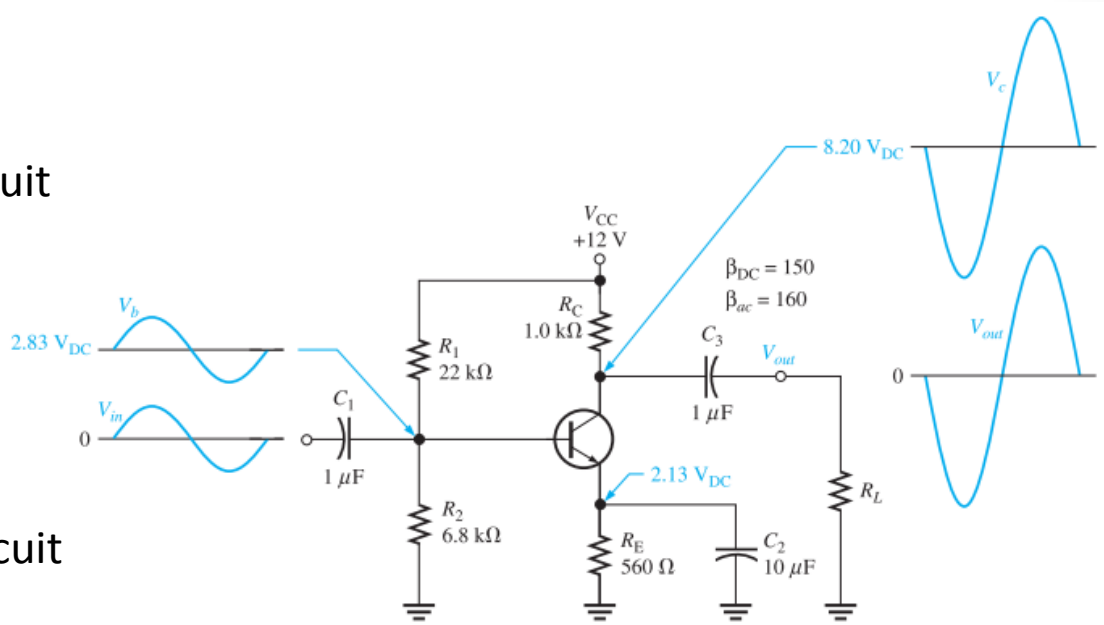
C.E. AC Analysis

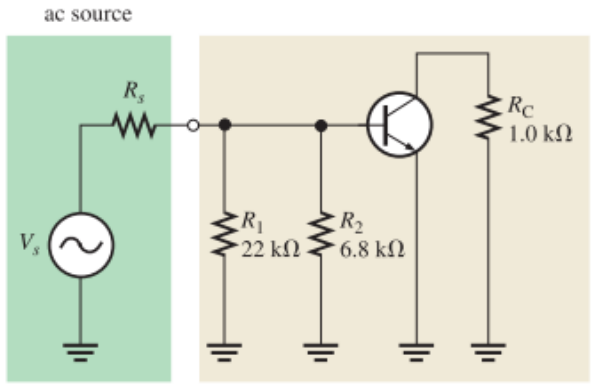
- **DC Analysis:**

Capacitors → Open Circuit
(See before)

- **AC Analysis:**

Capacitors → short Circuit
DC supply → ground





AC r-parameter Model

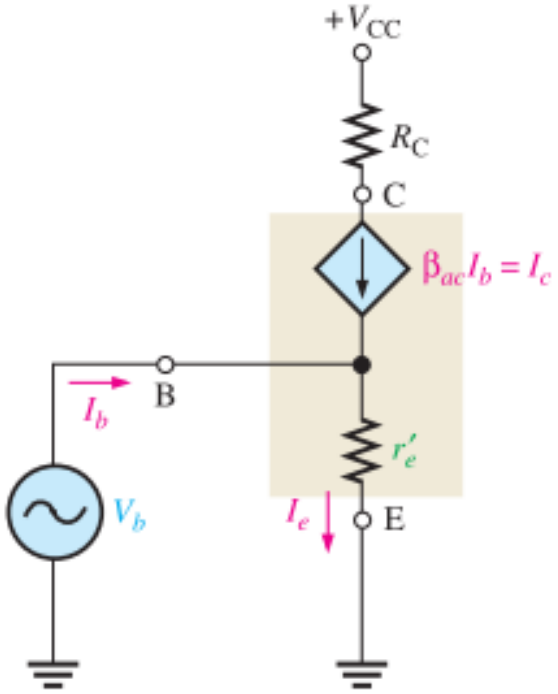
Input resistance $R_{in(base)} = \beta_{ac} r'_e$

Output resistance $R_{out} \cong R_C$

Voltage gain $A_v = \frac{R_C}{r'_e}$

Current gain $A_i = \frac{I_c}{I_s}$

Power gain $A_p = A'_v A_i$

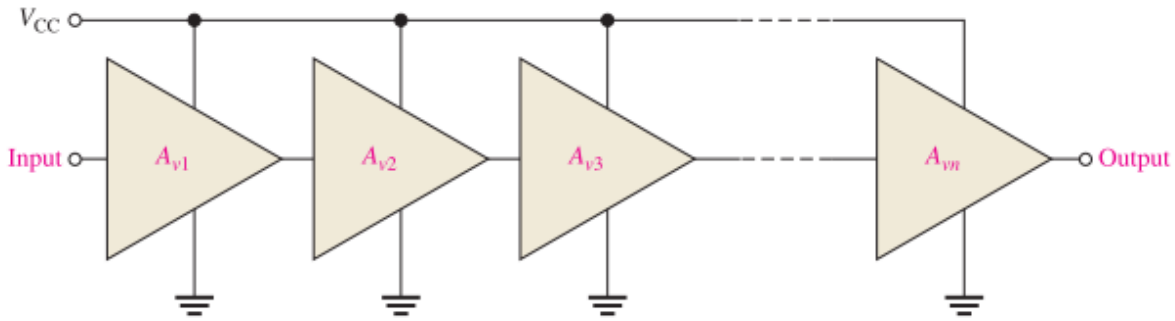


Multistage Amplifier

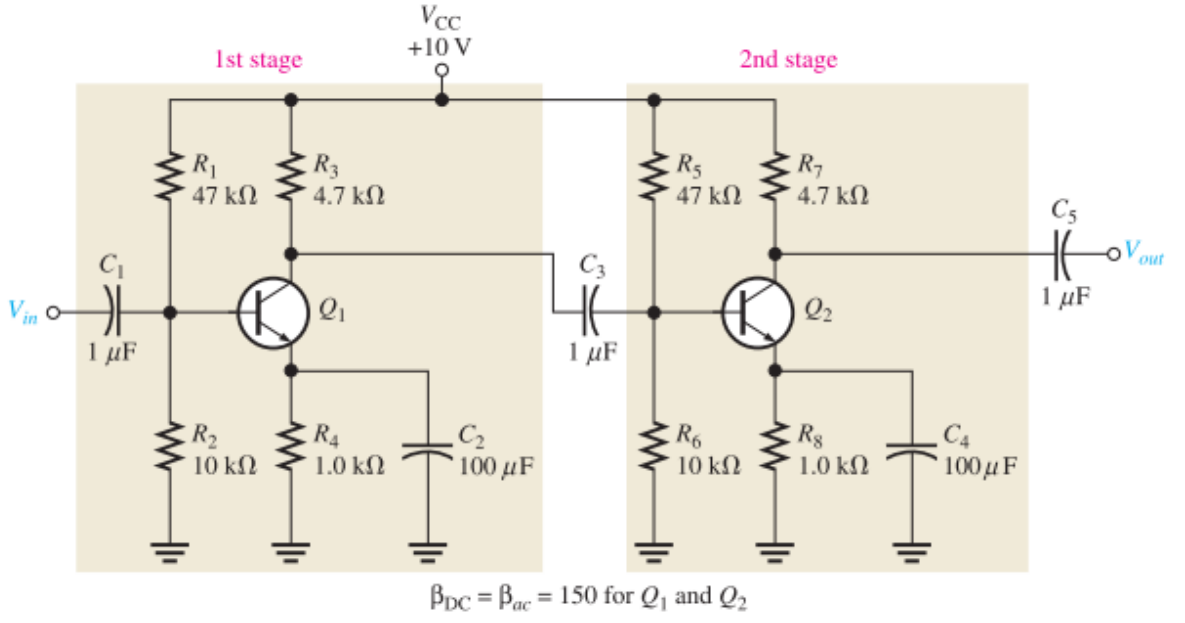
$$A_v' = A_{v1}A_{v2}A_{v3}\ldots A_{vn}$$

$$A_{v(\text{dB})} = 20 \log A_v$$

$$A'_{v(\text{dB})} = A_{v1(\text{dB})} + A_{v2(\text{dB})} + \cdots + A_{vn(\text{dB})}$$



- A two-stage common-emitter amplifier.



FET vs. BJT

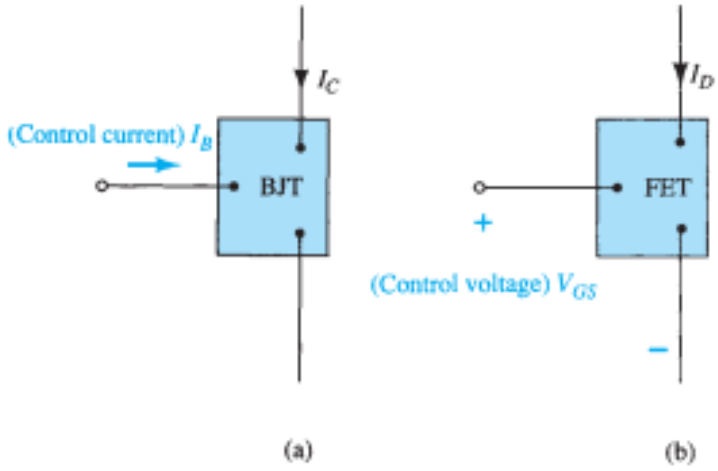
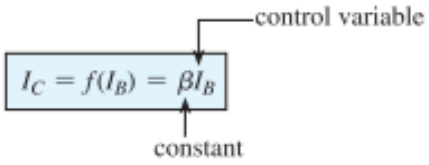


FIG. 6.1
(a) Current-controlled and (b) voltage-controlled amplifiers.

- One of the most important characteristics of the FET is its high input impedance.
- Typical ac voltage gains for BJT amplifiers are a great deal more than for FETs.
- FETs are more temperature stable than BJTs, and FETs are usually smaller than BJTs, making them particularly useful in integrated-circuit (IC) chips.

FET vs. BJT..



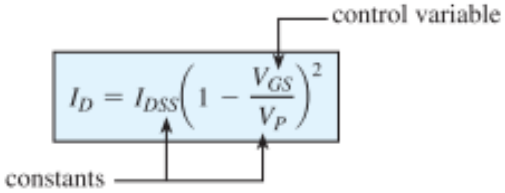


TABLE 6.2

JFET		*BJT*
$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$	$\Leftrightarrow$	$I_C = \beta I_B$
$I_D = I_S$	$\Leftrightarrow$	$I_C \cong I_E$
$I_G \cong 0\ \text{A}$	$\Leftrightarrow$	$V_{BE} \cong 0.7\ \text{V}$

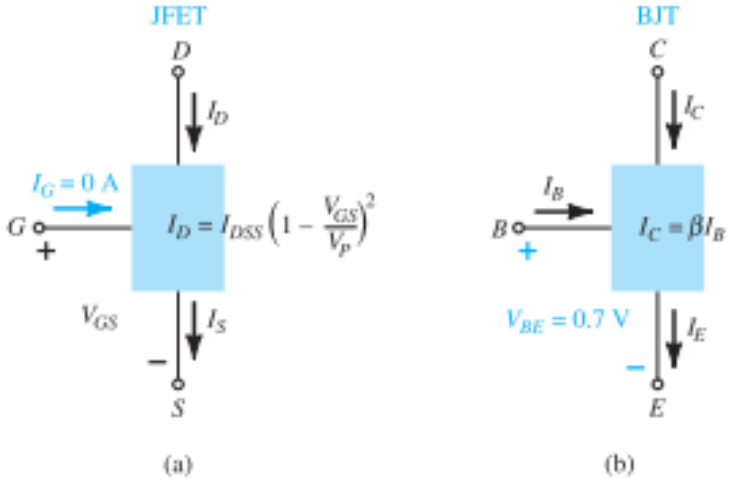


FIG. 6.23
(a) JFET versus (b) BJT.

FET Constructions

FIG. 6.4
Water analogy for the JFET control mechanism.

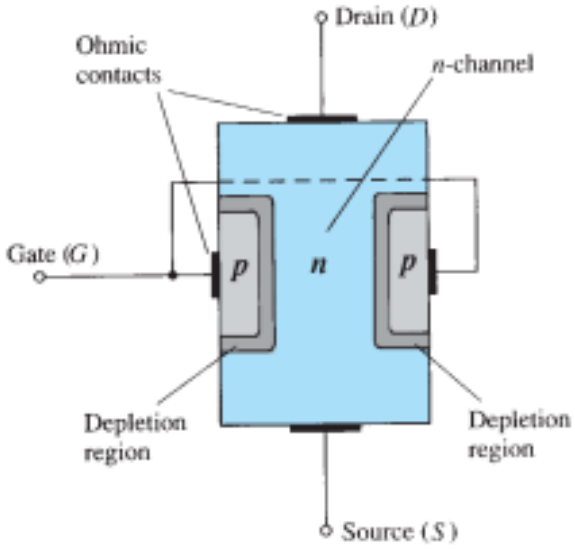


FIG. 6.3
Junction field-effect transistor (JFET).

FET Characteristics

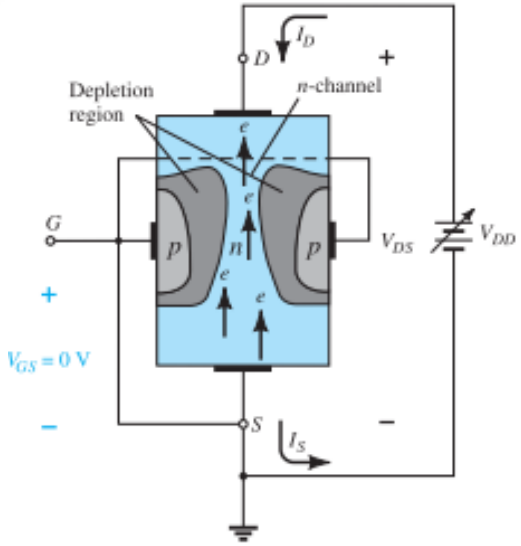


FIG. 6.5
JFET at $V_{GS} = 0$ V and $V_{DS} > 0$ V.

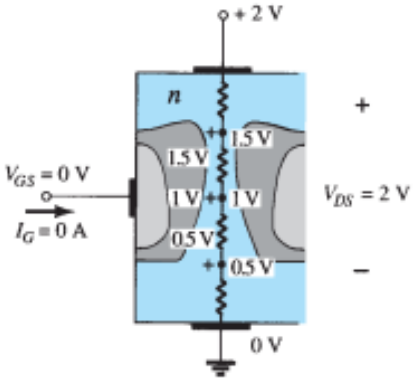


FIG. 6.6
Varying reverse-bias potentials across the p–n junction of an n-channel JFET.

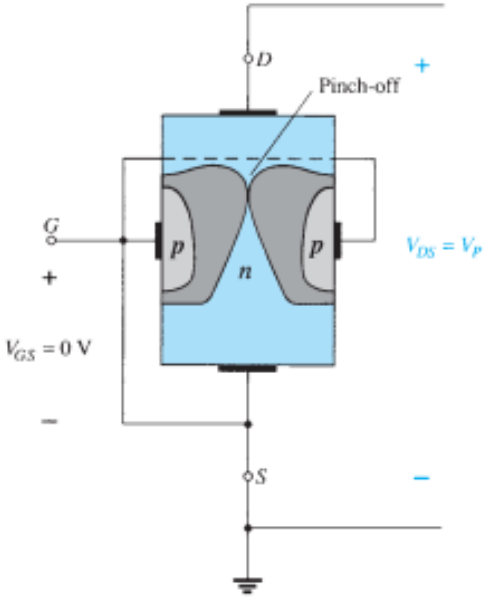
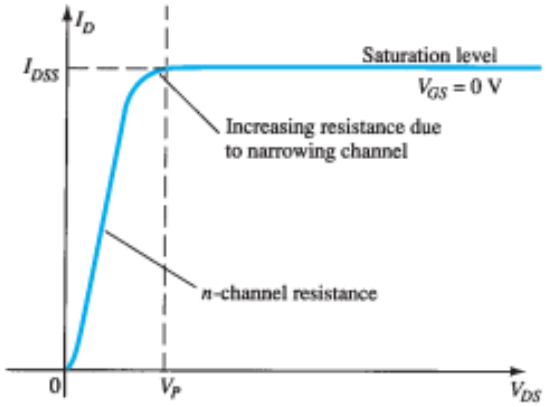


FIG. 6.8
Pinch-off ($V_{GS} = 0$ V, $V_{DS} = V_P$).



JFET & MOSFET Symbol

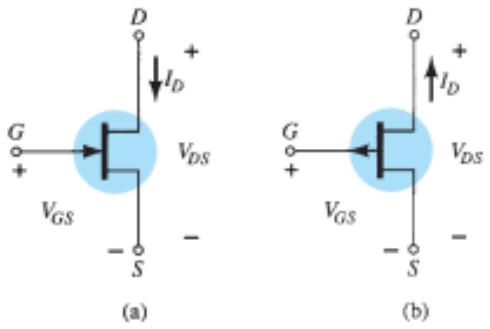


FIG. 6.14

JFET symbols: (a) n-channel; (b) p-channel.

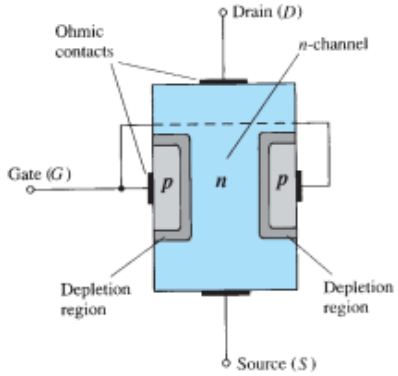


FIG. 6.3

Junction field-effect transistor (JFET).

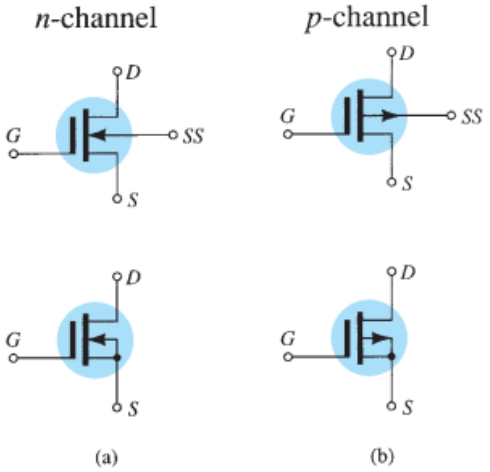


FIG. 6.30

Graphic symbols for: (a) n-channel depletion-type MOSFETs and (b) p-channel depletion-type MOSFETs.

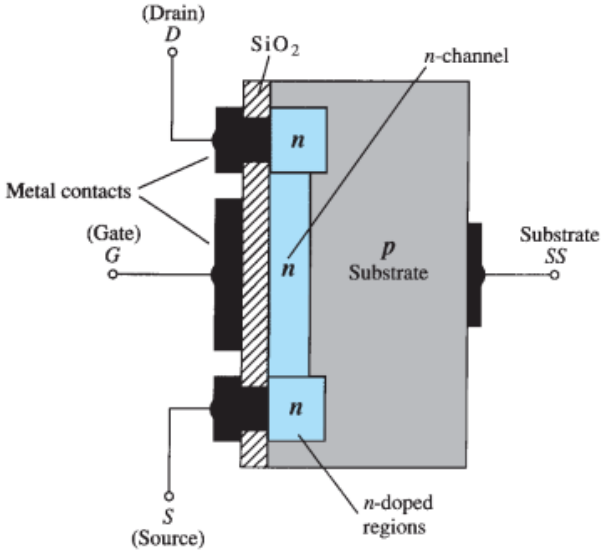


FIG. 6.24

n-Channel depletion-type MOSFET.

Other MOSFETS

- VMOS AND UMOS POWER MOSFETs

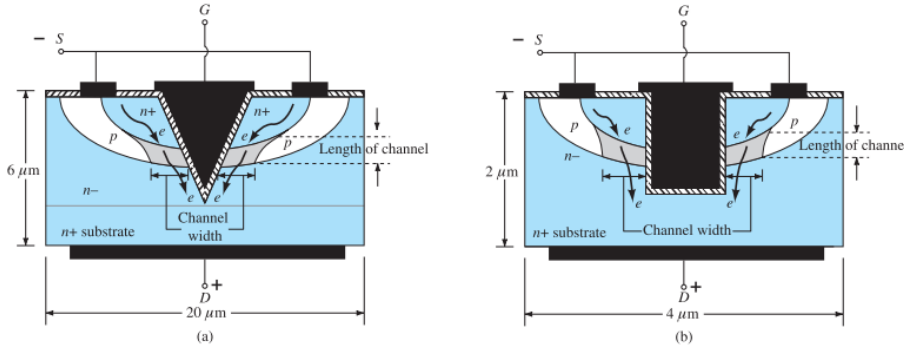


FIG. 6.43
(a) VMOS MOSFET; (b) UMOS MOSFET.

- CMOS

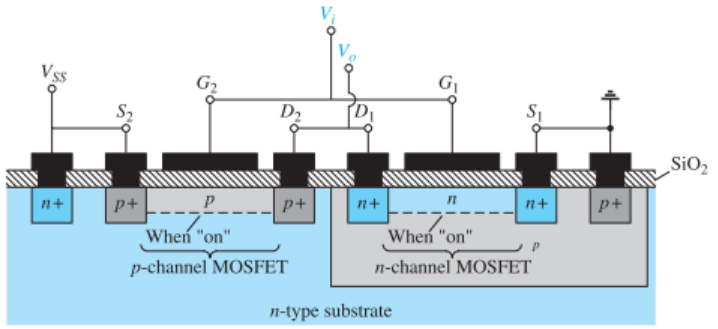


FIG. 6.44
CMOS with the connections indicated in Fig. 6.45.

- MESFET

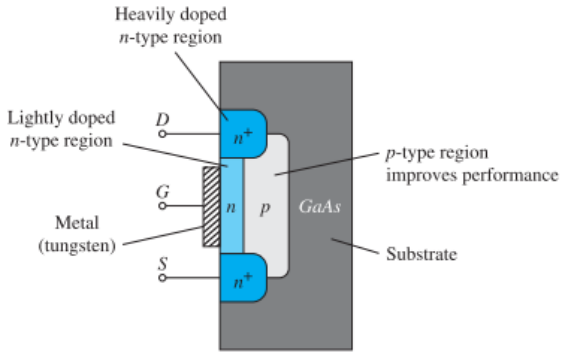


FIG. 6.47
Basic construction of an n-channel MESFET.

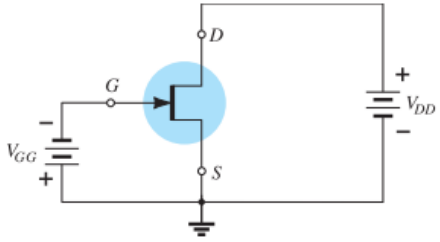


FIG. 6.49
Symbol and basic biasing arrangement for an n-channel MESFET.

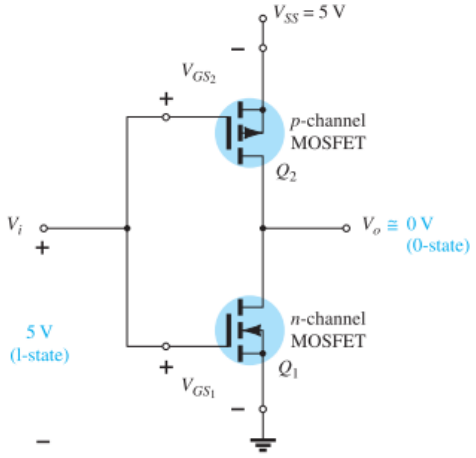
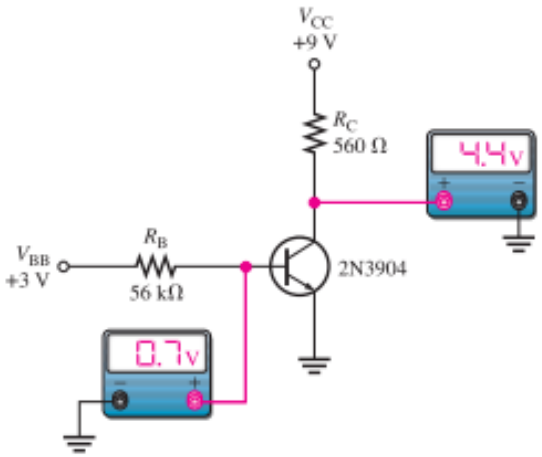


FIG. 6.45
CMOS inverter.

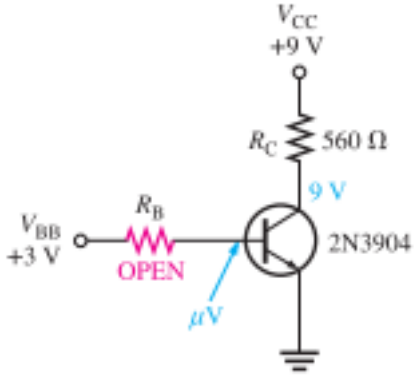
TROUBLESHOOTING

Testing with DMM

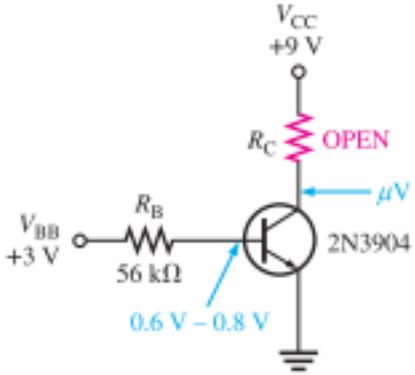


▲ FIGURE 4–38

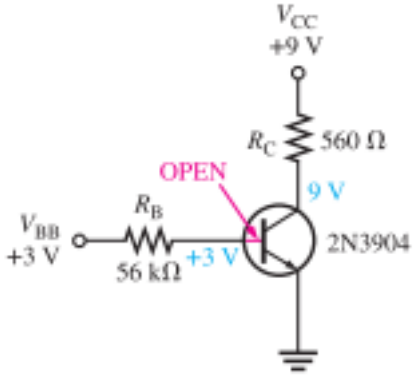
A basic transistor bias circuit.



(a) ***Fault:*** Open base resistor.
Symptoms: Readings from μV to a few mV at base due to floating point. 9 V at collector because transistor is in cutoff.

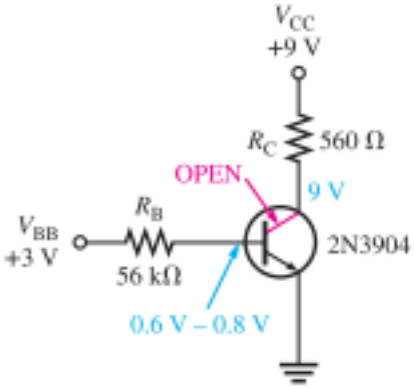


(b) ***Fault:*** Open collector resistor.
Symptoms: A very small voltage may be observed at the collector when a meter is connected due to the current path through the BC junction and the meter resistance.

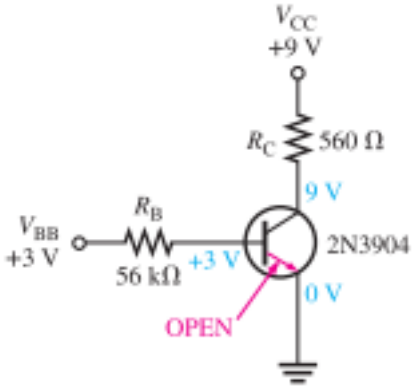


(c) ***Fault:*** Base internally open.
Symptoms: 3 V at base lead. 9 V at collector because transistor is in cutoff.

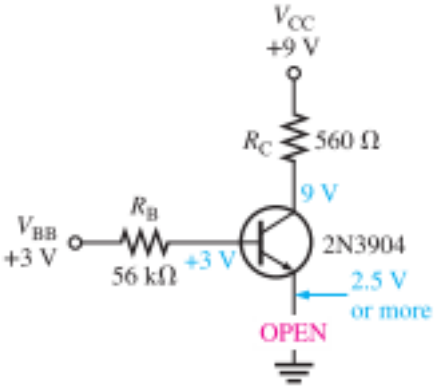
Testing with DMM..



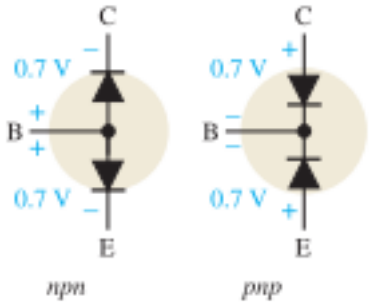
(d) ***Fault:*** Collector internally open. ***Symptoms:*** 0.6 V – 0.8 V at base lead due to forward voltage drop across base-emitter junction. 9 V at collector because the open prevents collector current.



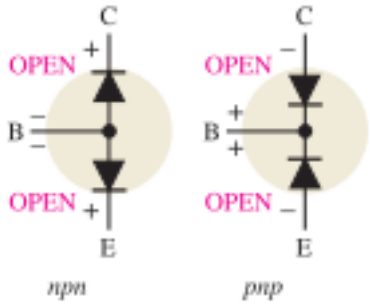
(e) ***Fault:*** Emitter internally open. ***Symptoms:*** 3 V at base lead. 9 V at collector because there is no collector current. 0 V at the emitter as normal.



(f) ***Fault:*** Open ground connection. ***Symptoms:*** 3 V at base lead. 9 V at collector because there is no collector current. 2.5 V or more at the emitter due to the forward voltage drop across the base-emitter junction. The measuring voltmeter provides a forward current path through its internal resistance.

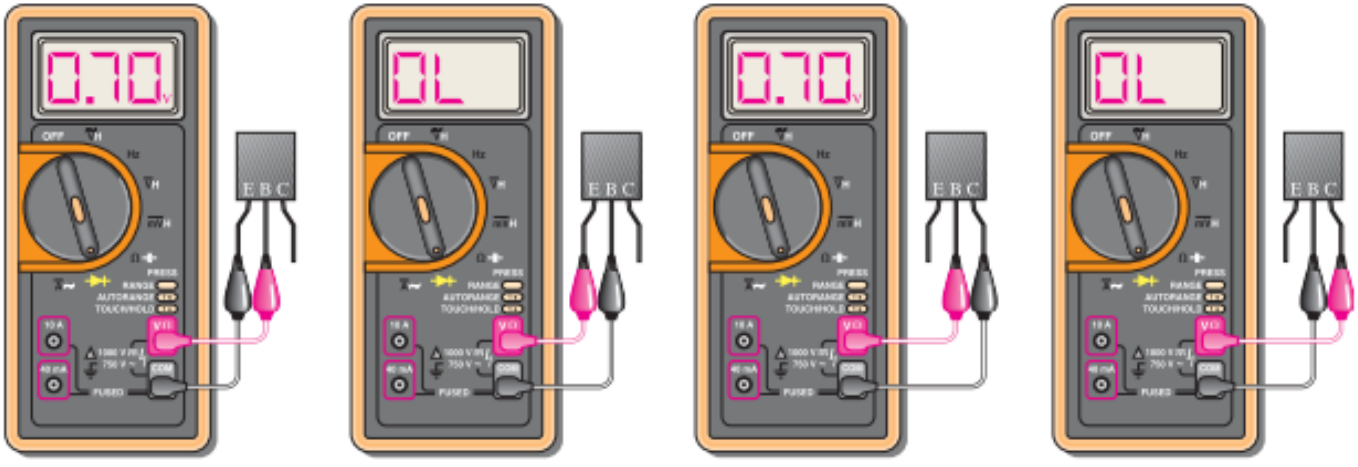


(a) Both junctions should typically read 0.7 V when forward-biased.



(b) Both junctions should ideally read OPEN when reverse-biased.

Testing with DMM...



(a) Forward-bias test of the BE junction

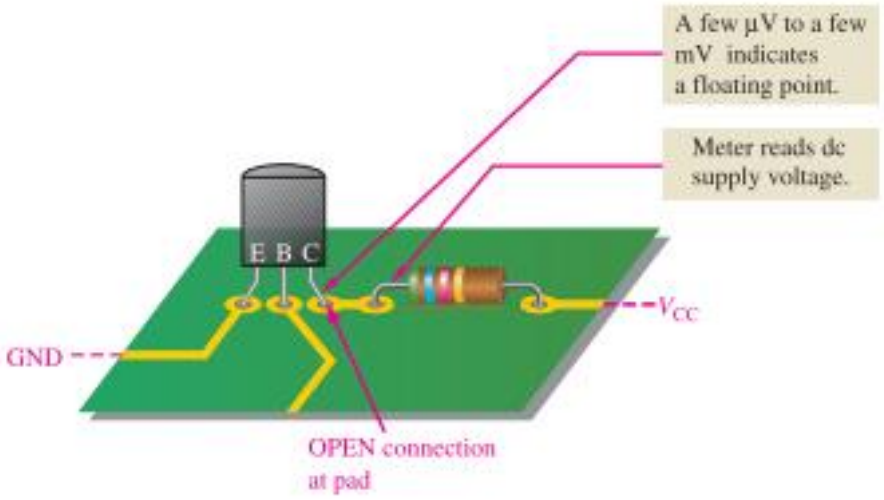
(b) Reverse-bias test of the BE junction

(c) Forward-bias test of the BC junction

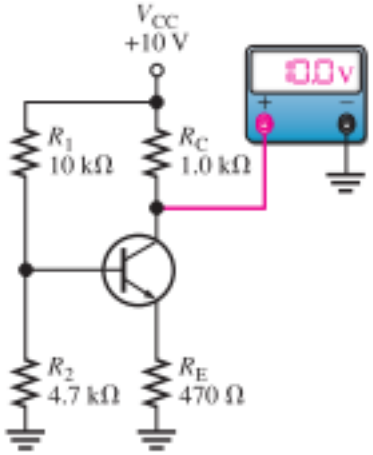
(d) Reverse-bias test of the BC junction

▲ FIGURE 4–41

Typical DMM test of a properly functioning *npn* transistor. Leads are reversed for a *pnp* transistor.



Voltage Divider circuit



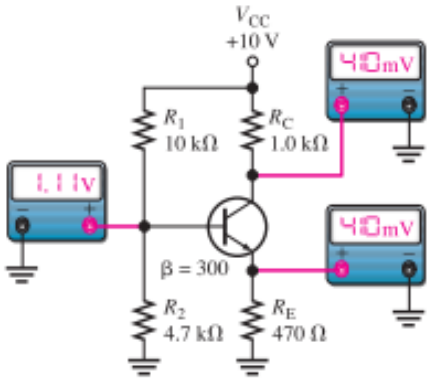
(a) Faulty circuit

FAULT	DESCRIPTION	V_C	V_E	V_B
1	R_1 open	10 V	0 V	0 V
2	R_E open	10 V	2.50 V	3.20 V
3	Base internally open	10 V	0 V	3.20 V
4	Emitter internally open	10 V	0 V	3.20 V
5	Collector internally open	10 V	0.41 V	1.11 V

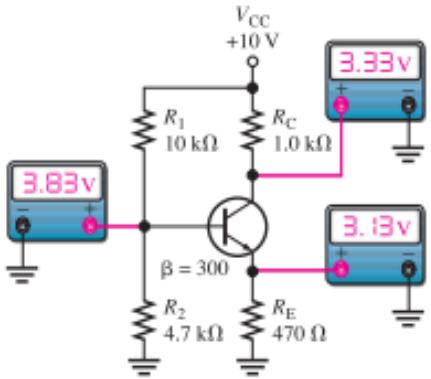
(b) Possible faults for circuit in part (a)

▲ **FIGURE 5–25**

Faults for which $V_C = V_{CC}$.



(a) R_C open



(b) R_2 open

◀ **FIGURE 5–27**

Faults for which the transistor is conducting or appears to be conducting.

2-stage Amplifier

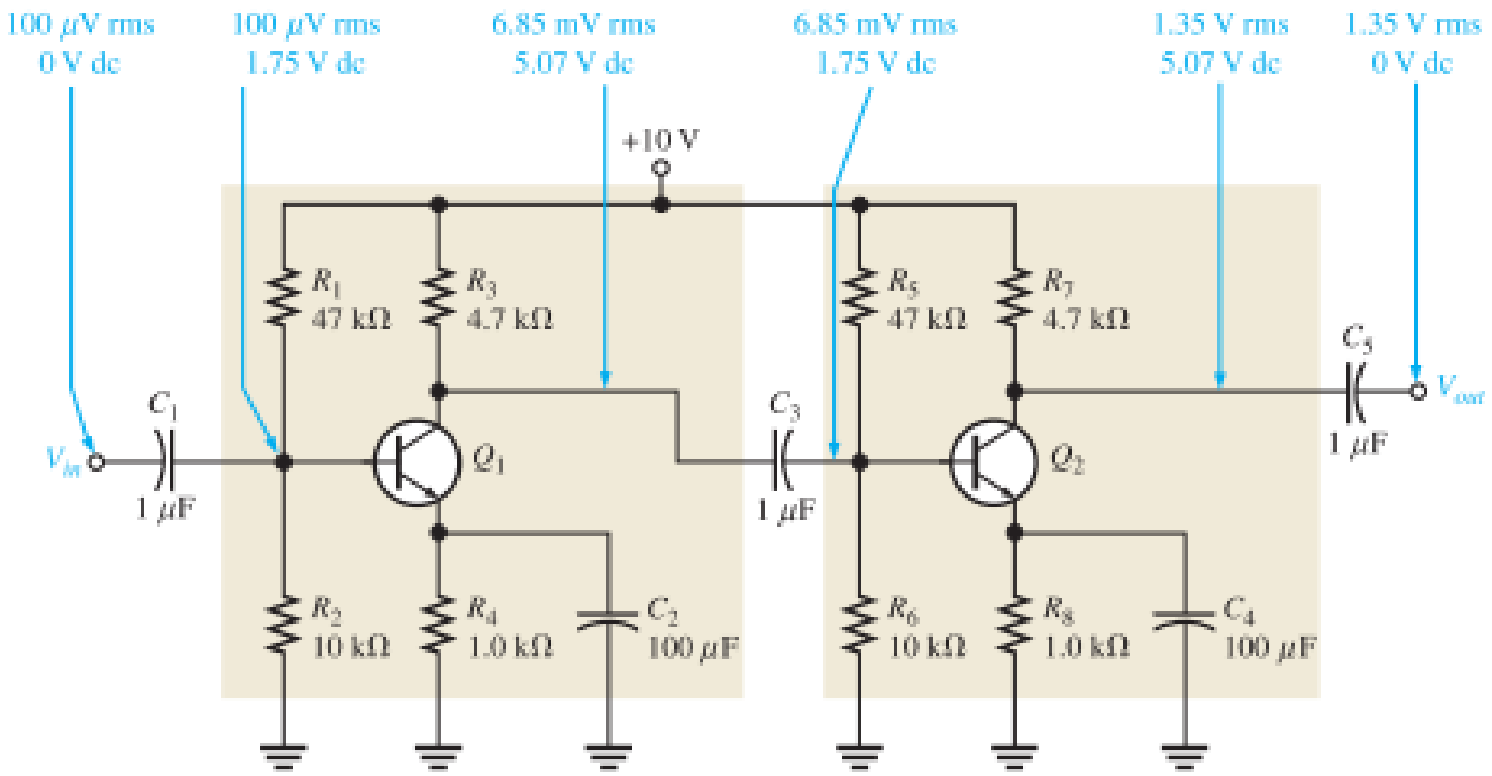


FIGURE 6–42

A two-stage common-emitter amplifier with correct voltages indicated. Both transistors have dc and ac betas of 150. Different values of β will produce slightly different results.

FET circuits

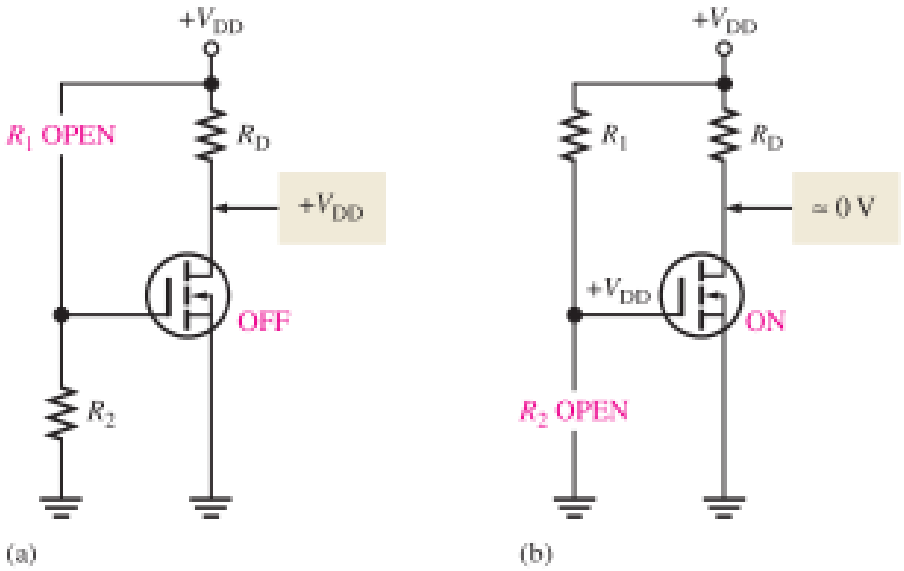


FIGURE 8–56

Failures in an E-MOSFET circuit with voltage-divider bias.

PRACTICAL APPLICATIONS

Relay Driver

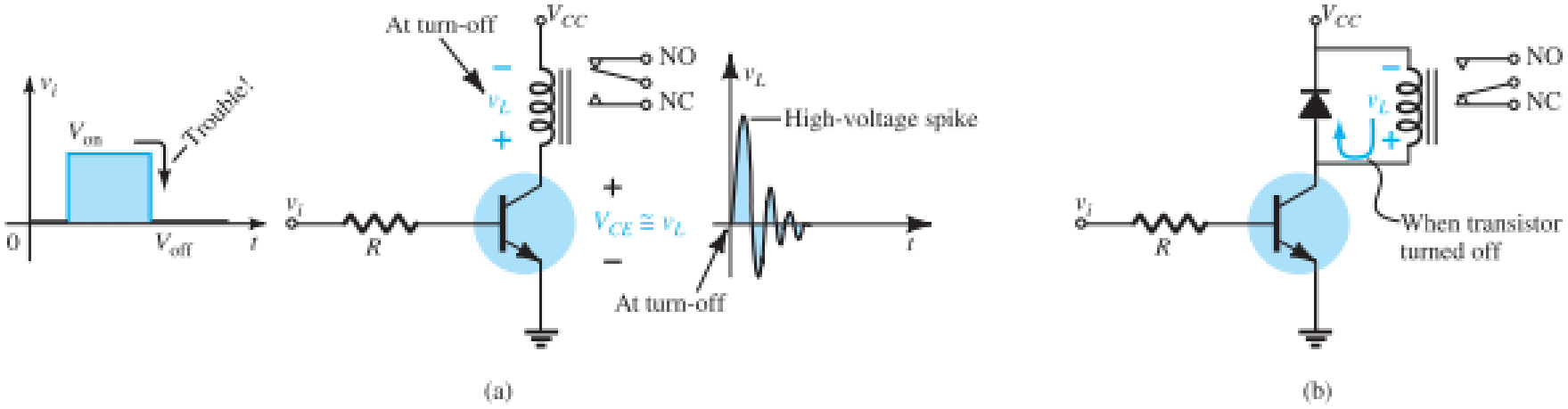


FIG. 4.104

Relay driver: (a) absence of protective device; (b) with a diode across the relay coil.

Light Control

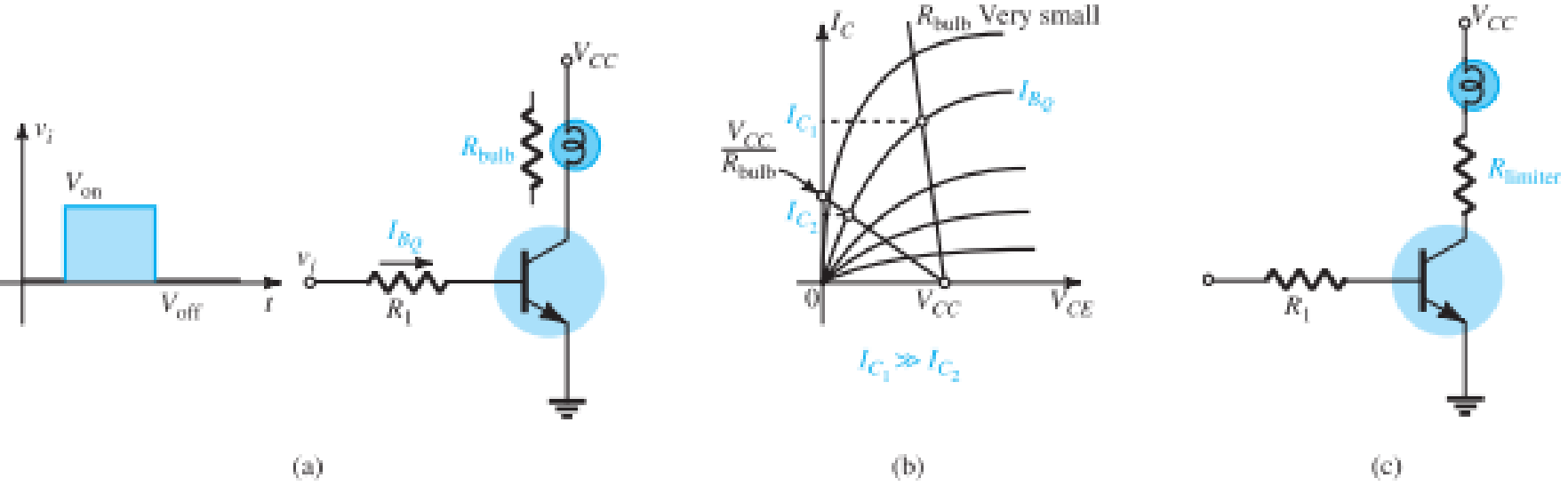


FIG. 4.105

Using the transistor as a switch to control the on–off states of a bulb: (a) network; (b) effect of low bulb resistance on collector current; (c) limiting resistor.

Maintaining fixed load current

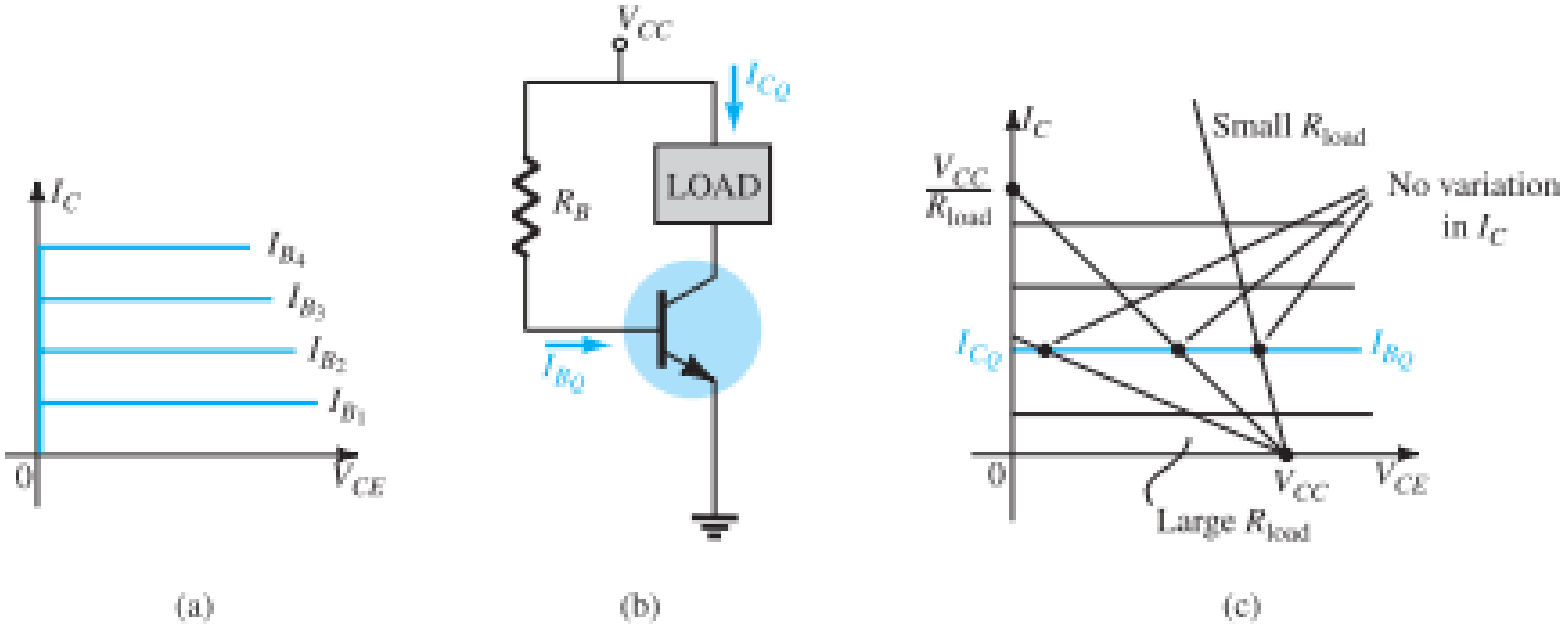


FIG. 4.106

Building a constant-current source assuming ideal BJT characteristics: (a) ideal characteristics; (b) network; (c) demonstrating why I_C remains constant.

Alarm System

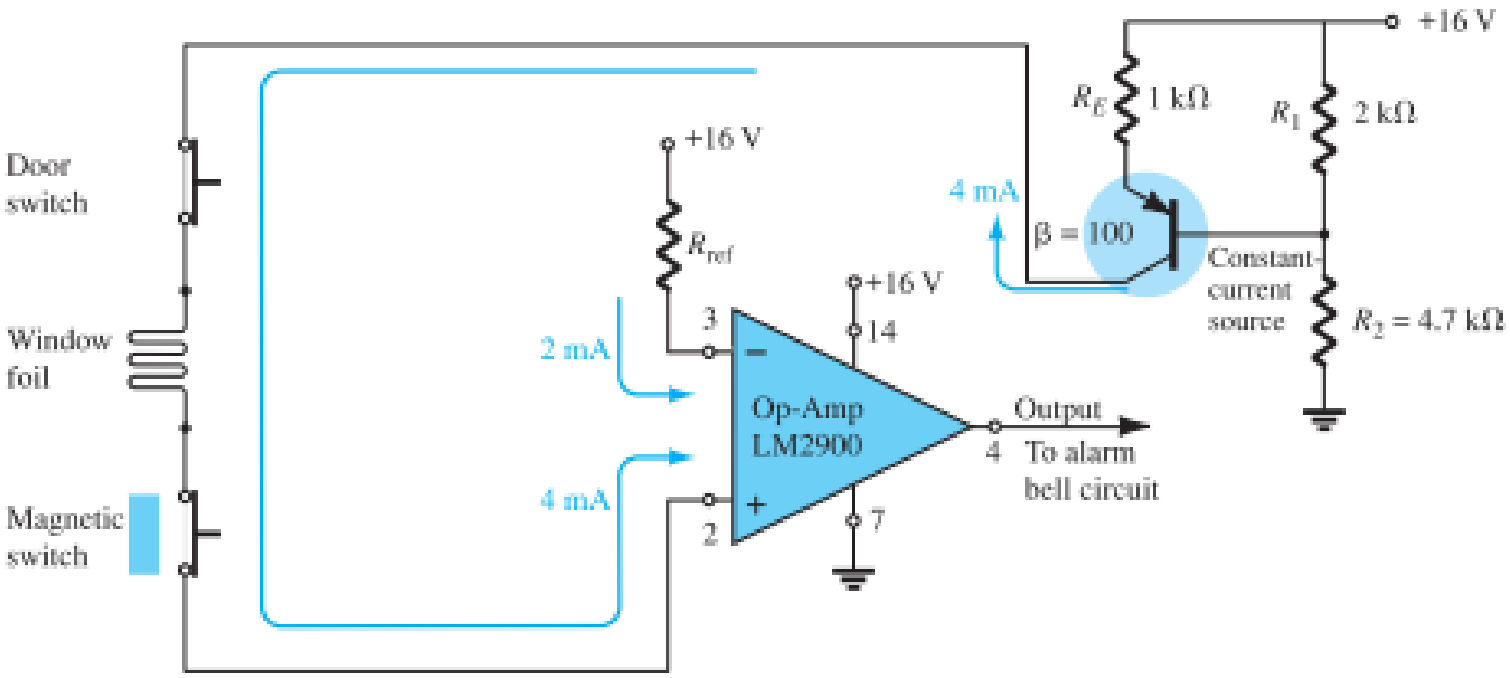


FIG. 4.108

An alarm system with a constant-current source and an op-amp comparator.

Logic gates

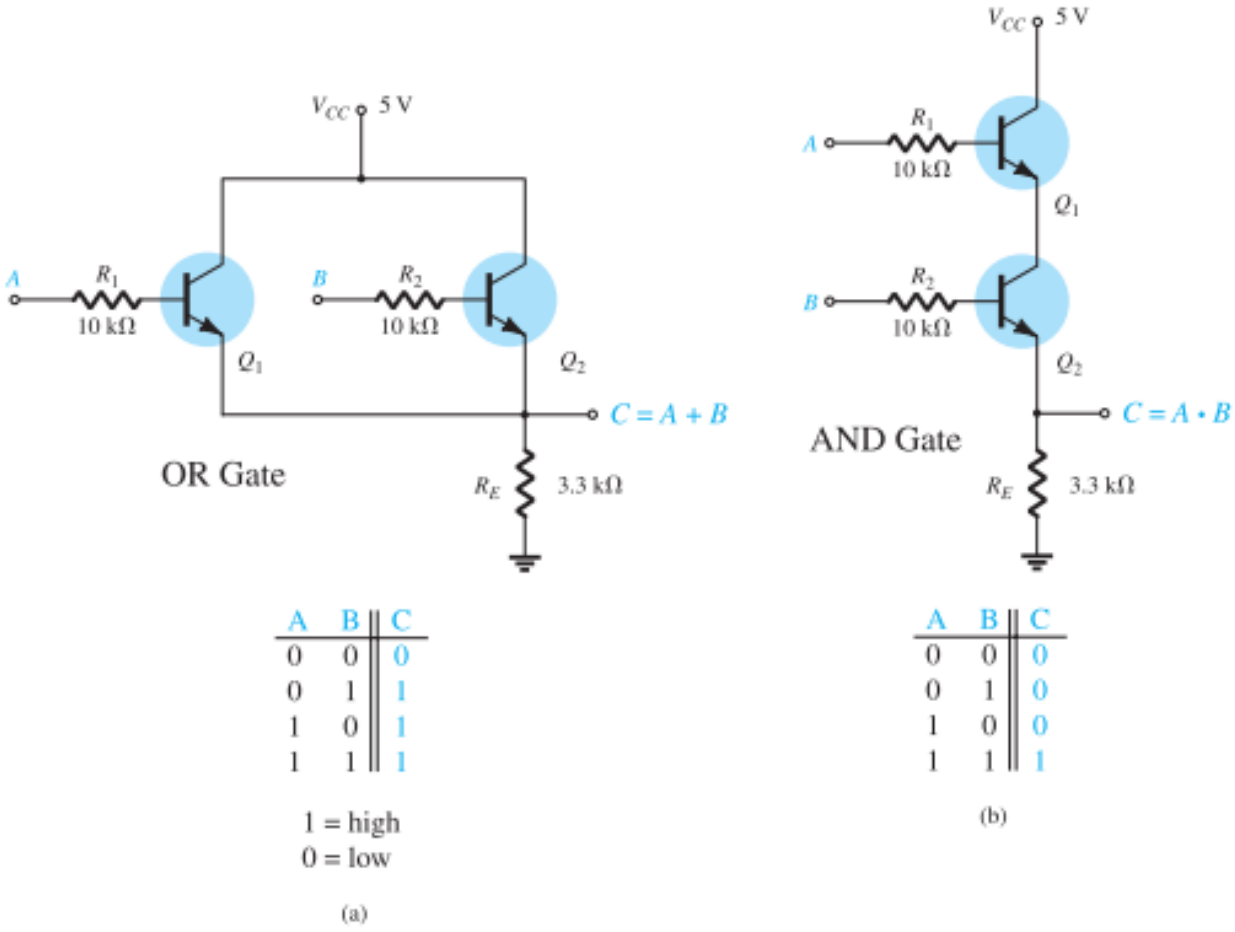


FIG. 4.111
BJT logic gates: (a) OR; (b) AND.

Voltage level indicator

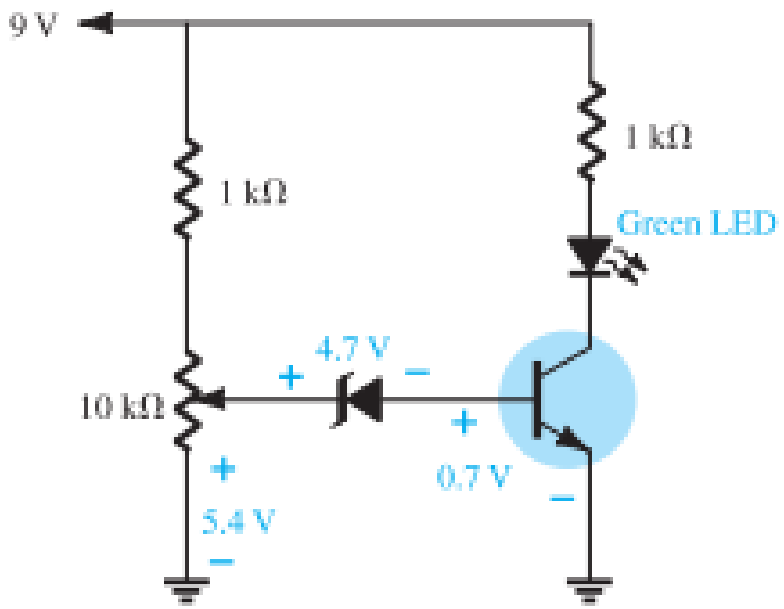


FIG. 4.112
Voltage level indicator.

Audio Mixer

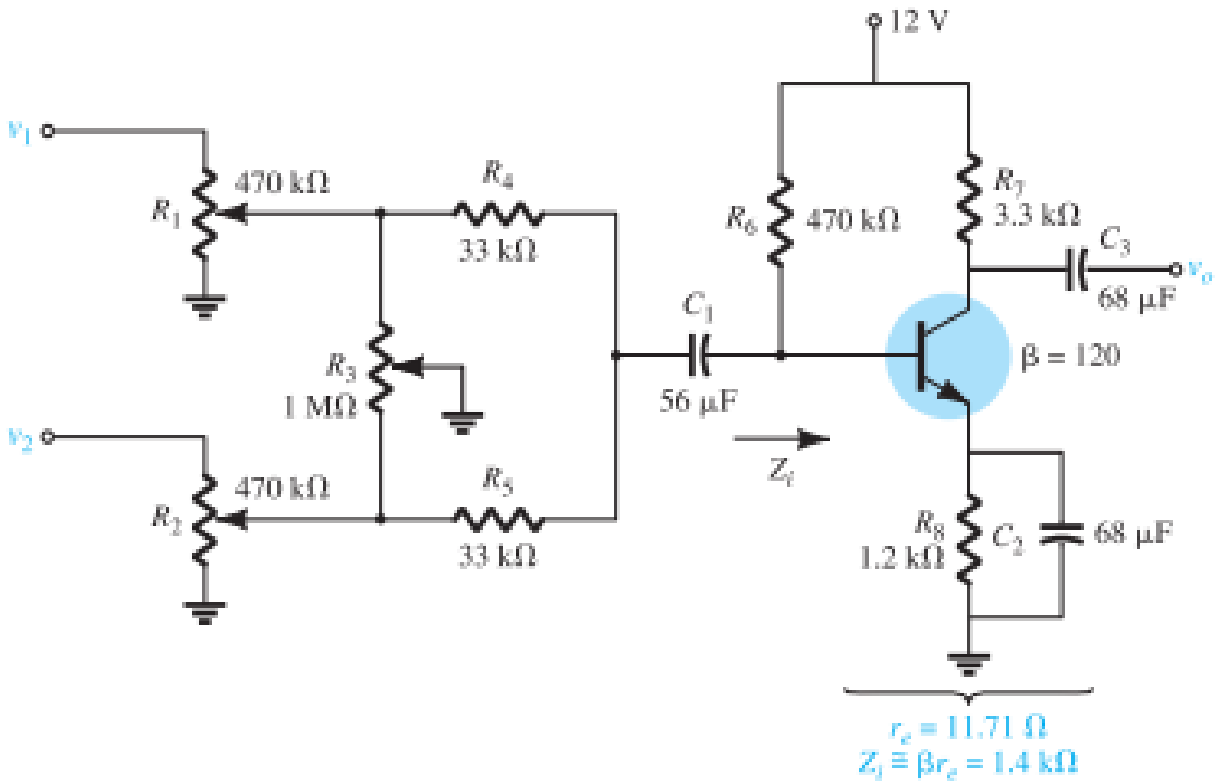


FIG. 5.130
Audio mixer.

Preamplifier

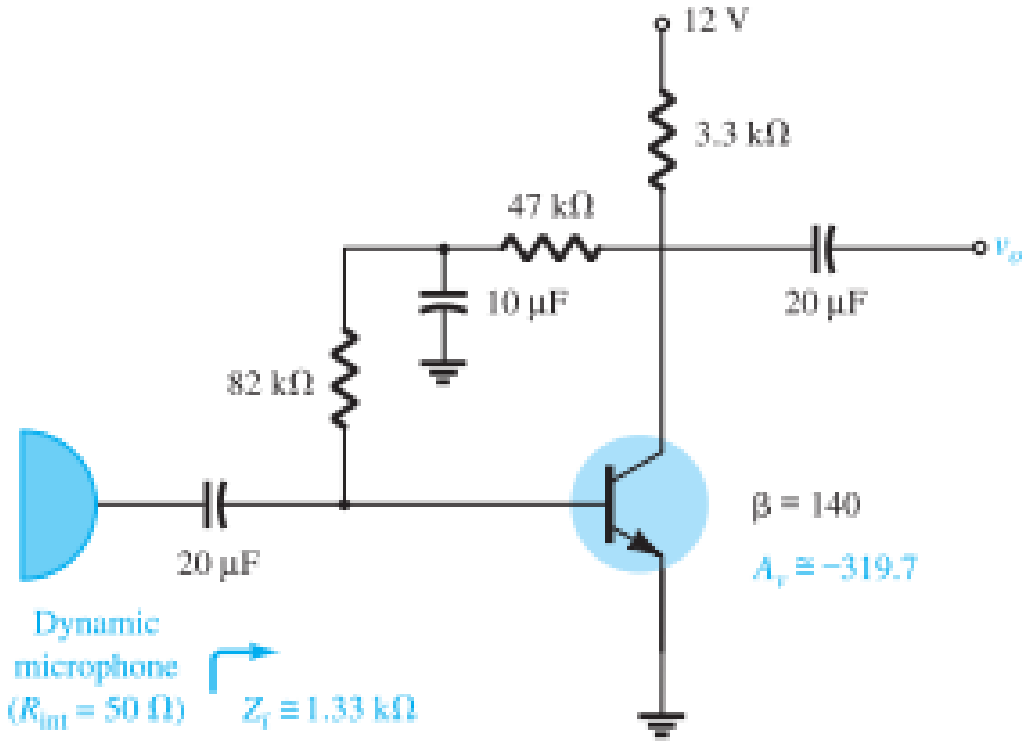


FIG. 5.133

Preamplifier for a dynamic microphone.

Voltage controlled resistor

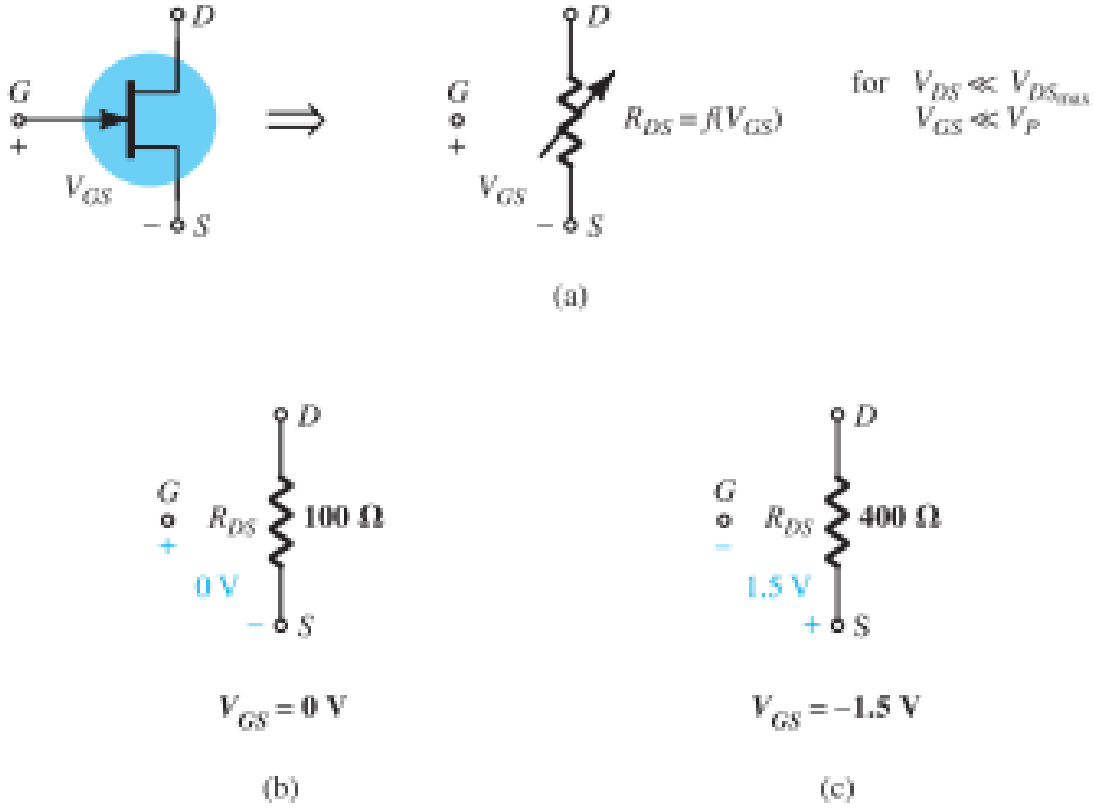
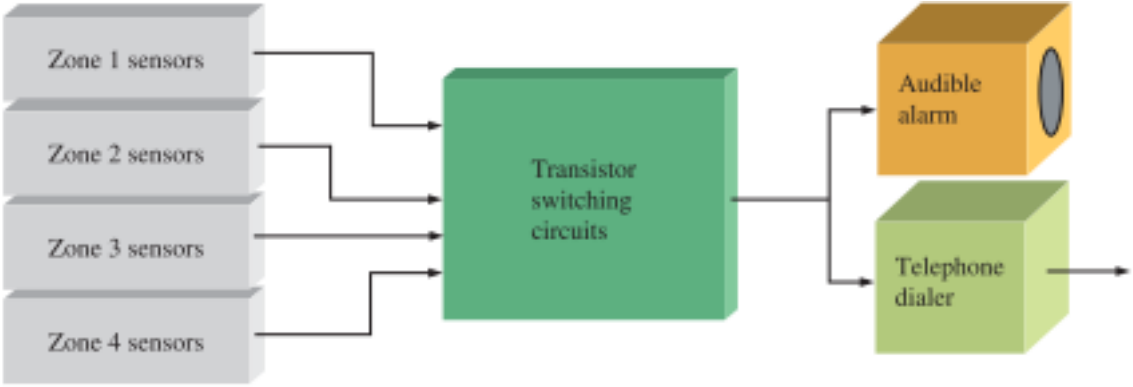
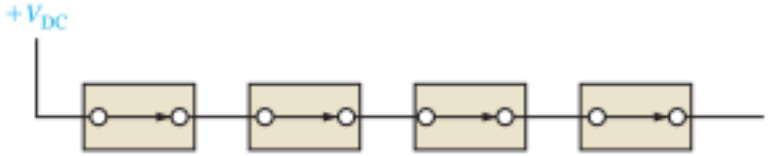


FIG. 7.64

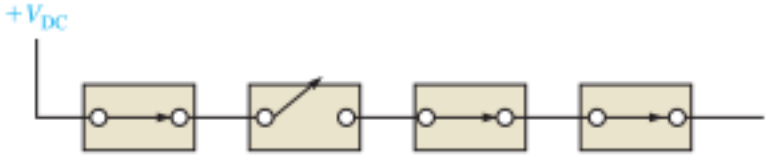
JFET voltage-controlled drain resistance: (a) general equivalence; (b) with $V_{GS} = 0$ V; (c) with $V_{GS} = -1.5$ V.

Security Alarm System

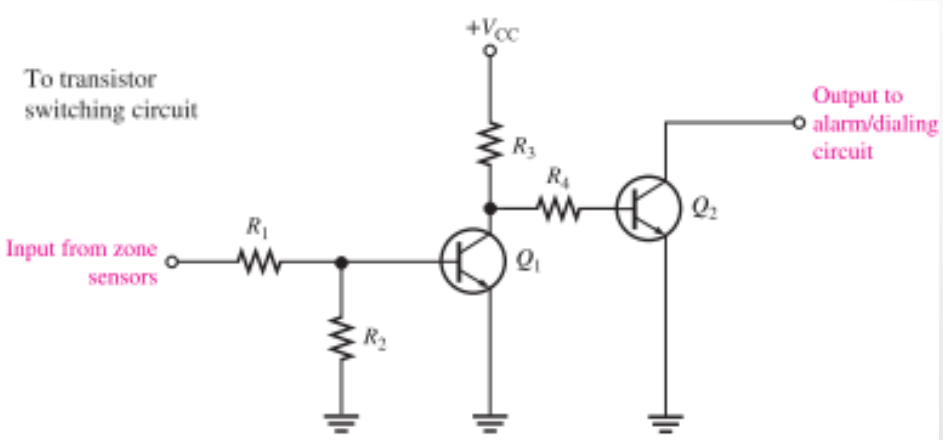




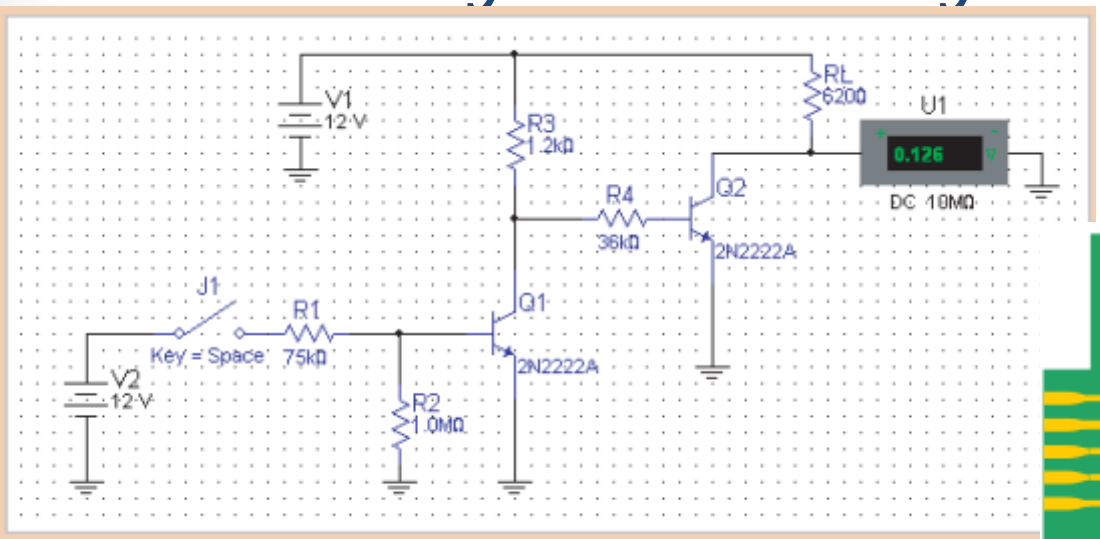
(a) Series zone sensors are normally closed.

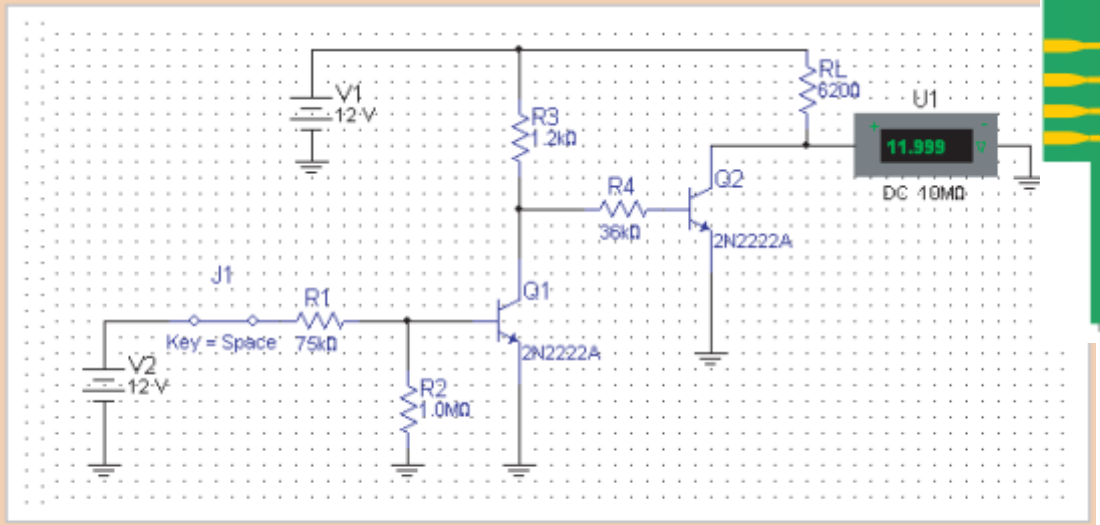


(b) Intrusion into the zone causes a sensor to open.

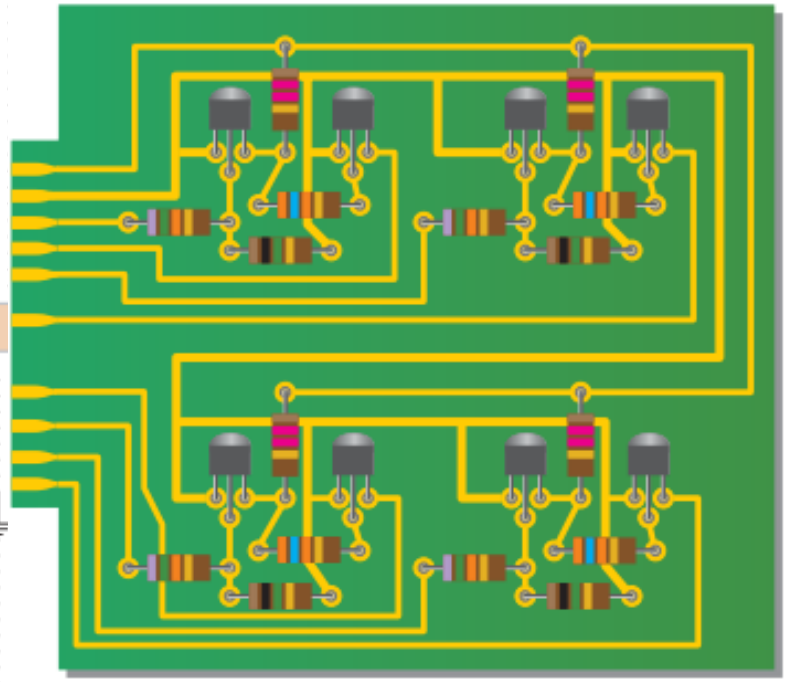


Security Alarm System..

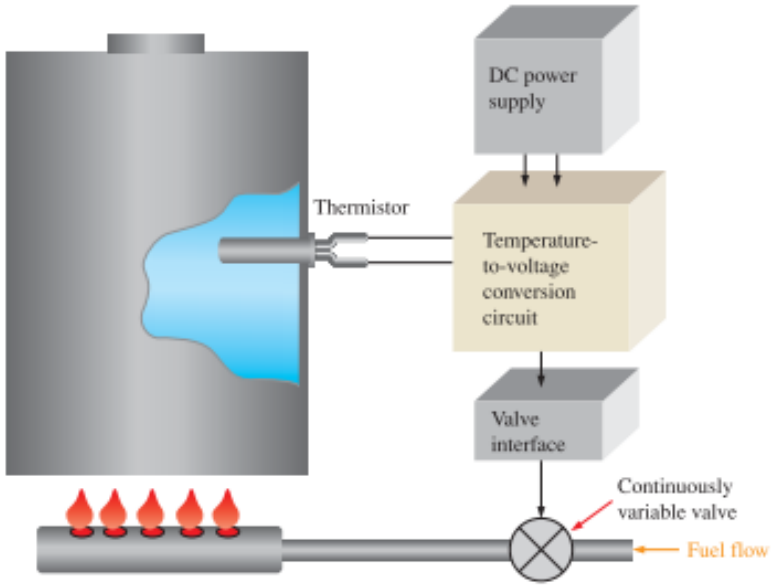


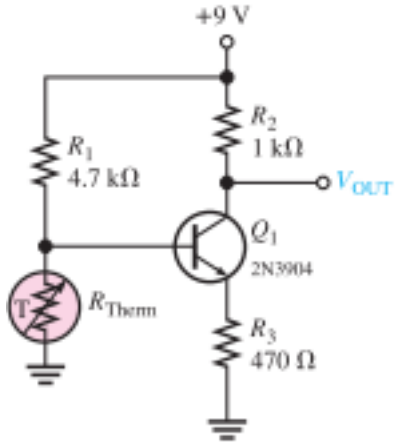


▲ FIGURE 4–51
Simulation of the switching circuit.



Temperature to Voltage Converter



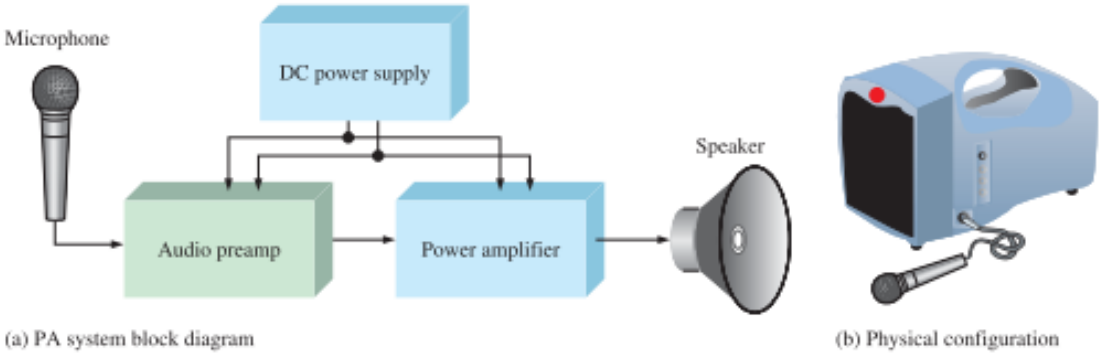


(a) Circuit

TEMPERATURE, °C	THERMISTOR RESISTANCE, kΩ
60	1.256
65	1.481
70	1.753
75	2.084
80	2.490

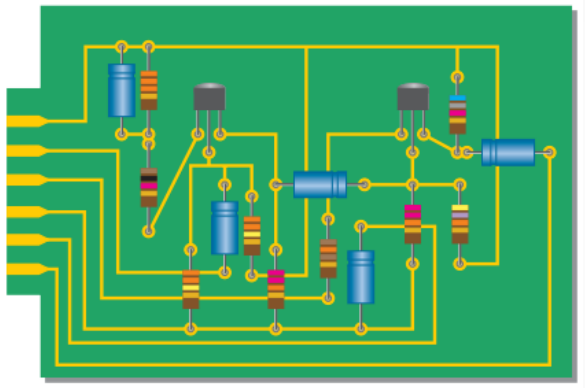
(b) Temperature characteristic of the thermistor for the specified range

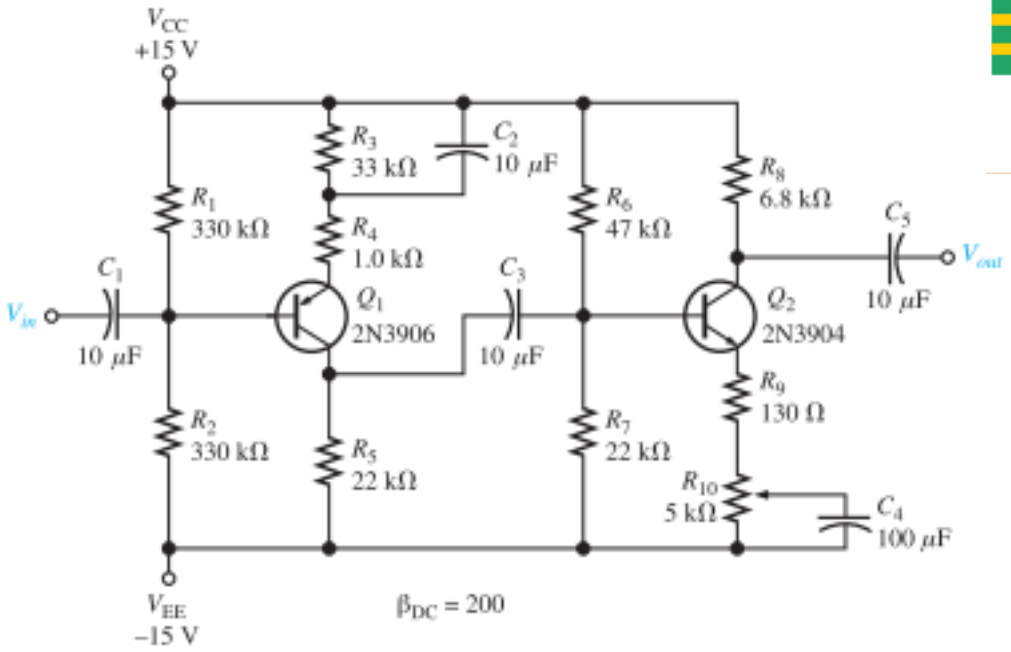
Audio Preamplifier



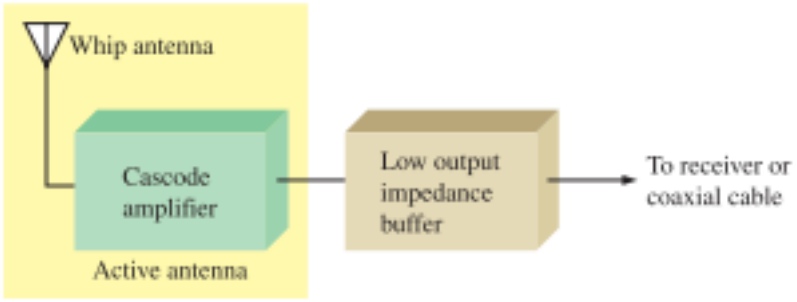
(a) PA system block diagram

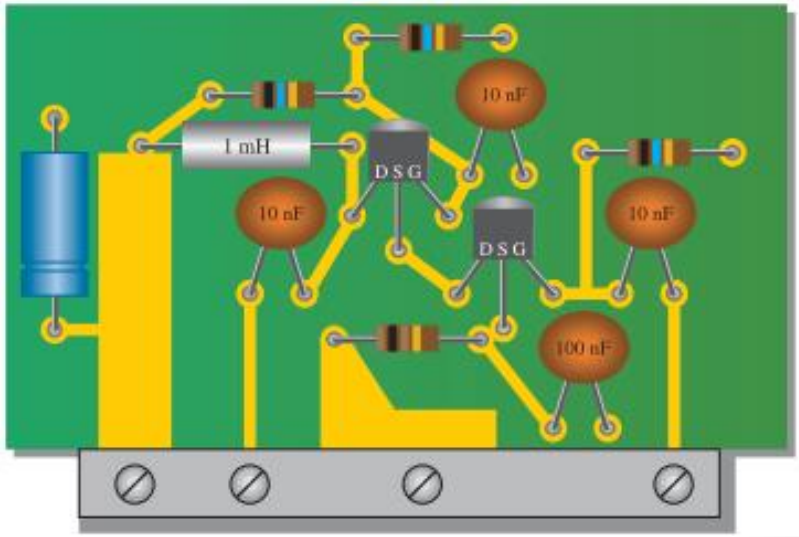
(b) Physical configuration

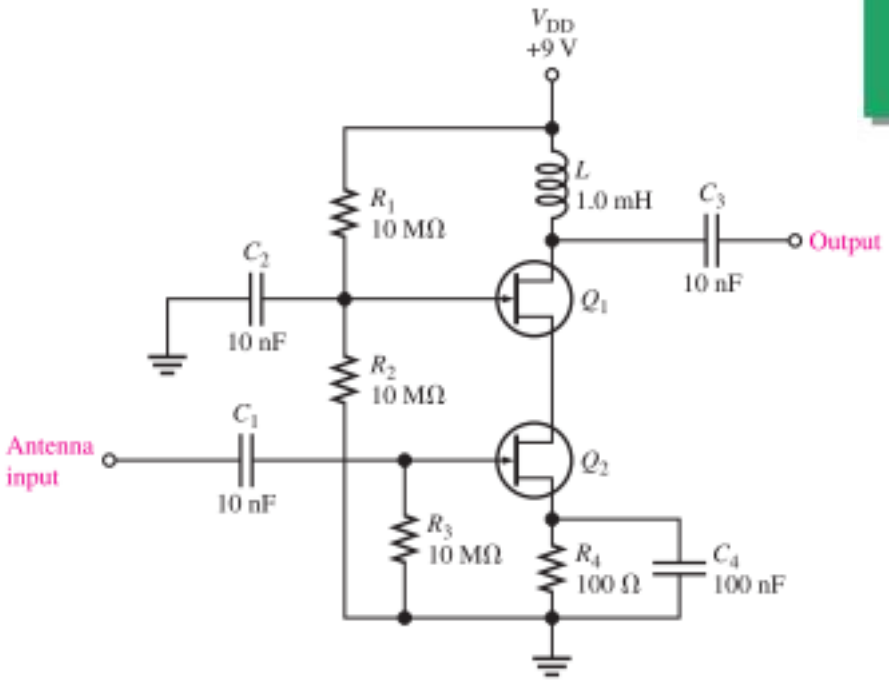




Active Antenna







References

- Floyd, chapters:4-6,8-9
- Boylestad, chapters: 3-8

- For enquires:
  - ahmad.elbanna@feng.bu.edu.eg